Ordering number : ENA1059

SANYO Semiconductors
DATA SHEET

LA72730

Monolithic Linear IC
For TV
Audio/Video Switch

Overview

The LA72730 is an Audio/Video Switch for TV.

Functions

- Audio : Possible to Change 4 Channel×2, ALC OUTPUT, 4dB Amplifier MONITOR OUTPUT
- Video : Possible to Change 4 Channel, 6dB Amplifier
- Control : I^2C (Slave address : 92h)

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	Pin 8	7.0	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	300	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-55 to +150	°C

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended operating voltage	V_{CC}	Pin 8	5.0	V
Operating voltage range	V_{CC} op	Pin 8	4.5 to 5.5	V

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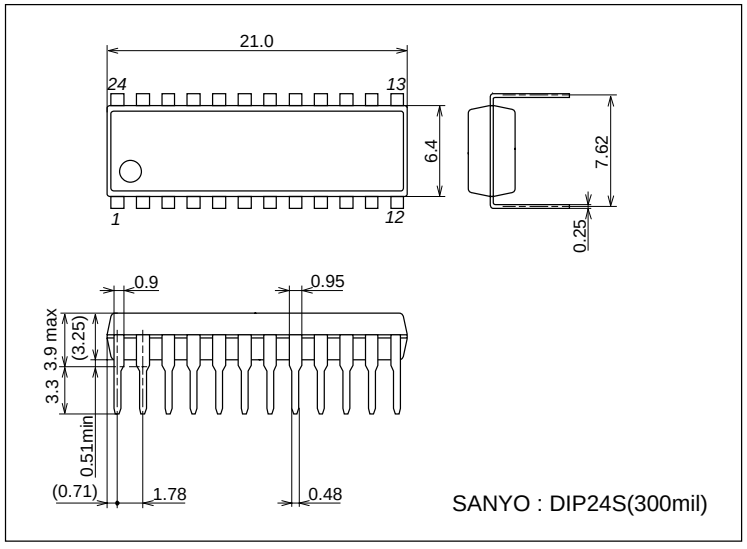
Electrical Characteristics at Ta = 25°C, V_{DD} = 5.0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current dissipation	I_{CC}	V_{CC} = 5V, No signal	15.2	18	20.8	mA
Audio block						
Audio input DC voltage	INa	No signal pin 1, 2, 3, 4, 5, 6, 23, 24 DC voltage	2.2	2.4	2.6	V
Audio output DC voltage	Oa	No signal pin 19, 20 DC voltage	2.2	2.4	2.6	V
Audio channel bandwidth	Fa	Input : 1kHz/20kHz, -6dBV : Pin 19, 20 output	-2	0	+2	dB
Audio voltage gain (Audio-out)	Aa1	f = 1kHz, V_{IN} = -6dBV, Pin 19, 20 output	-0.3	0.0	+0.3	dB
Audio voltage gain (Monitor-out)	Aa2	f = 1kHz, V_{IN} = -6dBV, Pin 12, 16 output	3.5	4.0	4.5	dB
Audio input dynamic range (Audio-out)	Da1	f = 1kHz, THD = ≤1% Pin 19, 20 output	-3.0	-1.0		dBV
Audio input dynamic range (Monitor-out)	Da2	f = 1kHz, THD = ≤1% Pin 13, 16 output	-5.0	-3.0		dBV
Audio channel PSRR	PSa	V_{CC} = 5V+1Vp-p, SINE WAVE (50Hz)	35	50		dB
Audio channel input impedance	Ria		80	100	120	kΩ
Audio channel output impedance	Roa		150	200	250	Ω
Audio channel crosstalk	CTa	f = 1kHz	65	80		dB
Audio channel S/N	SNa	Filter = DIN/AUDIO	70	85		dB
Audio channel THD	THDa	f = 1kHz, V_{IN} = -6dBV		0.15	0.3	%
ALC Detect level-1	ALC1		-10.5	-9	-7.5	dBV
ALC Detect level-2	ALC2		-15.5	-14	-12.5	dBV
ALC Detect level-3	ALC3		-13.5	-12	-10.5	dBV
ALC Detect level-4	ALC4		-19.5	-18	-16.5	dBV
Video block						
Video input DC voltage	INv		1.44	1.6	1.76	V
Video output DC voltage	Ov		1.26	1.4	1.54	V
Video channel bandwidth	Fv	-3dB frequency	10			MHz
Video signal voltage gain	Av	f = 500kHz, V_{IN} = 1Vp-p	5.0	6.0	7.0	dB
Video input dynamic range	Dv	f = 100kHz, THD ≤ 1%	2.0	2.5		Vp-p
Video channel PSRR	PSv	V_{CC} = 5V+1Vp-p, SINE WAVE (50Hz)	35	50		dB
Video channel input impedance	Riv		8.0	10	12.0	kΩ
Video channel output impedance	Rov		30	40	50	Ω
Video channel crosstalk	CTv	f = 3.58MHz, V_{IN} = 1Vp-p	45	60		dB
Video channel noise	SNv	Bandwidth 10MHz	55	60		dB

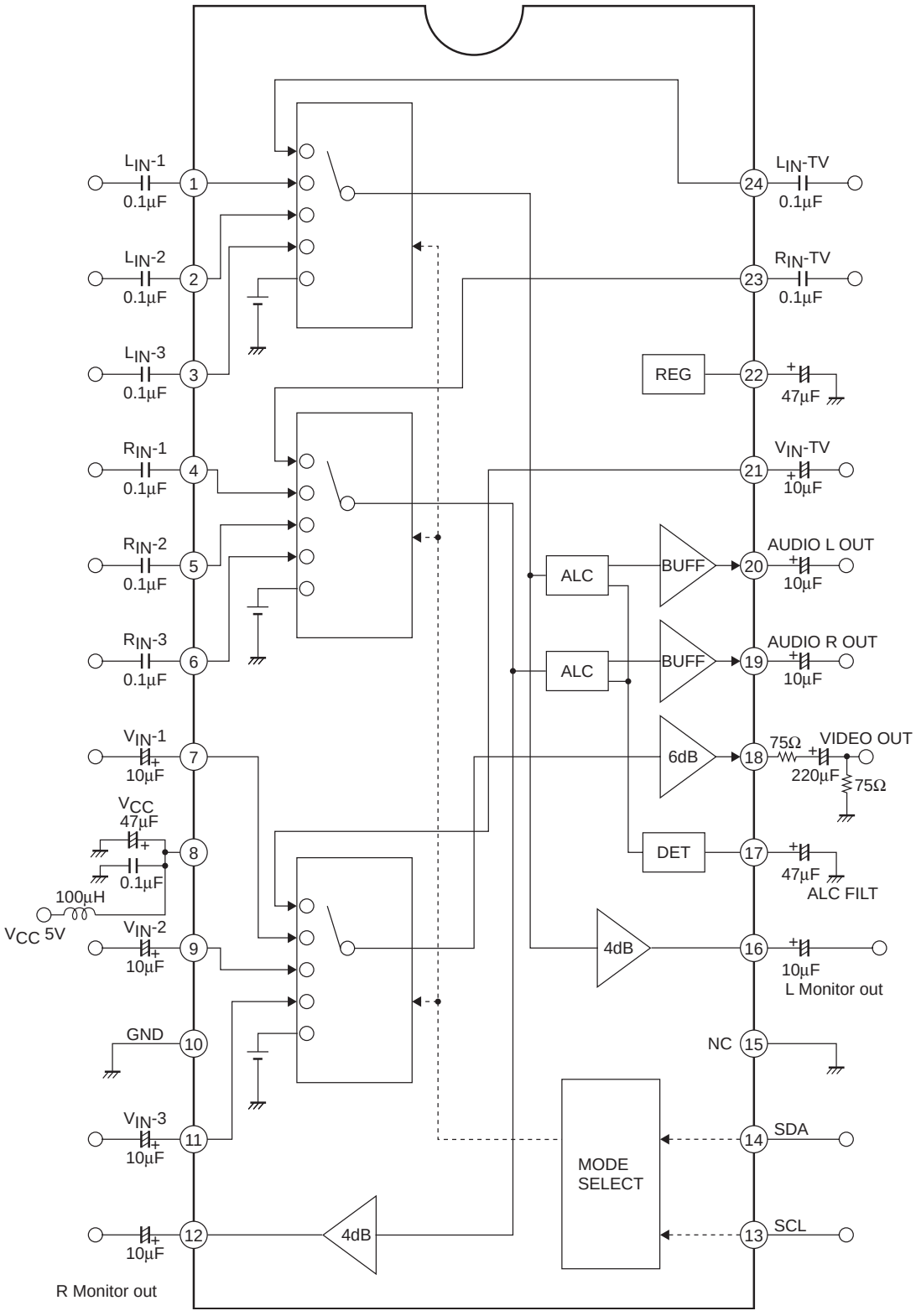
Package Dimensions

unit : mm (typ)

3067B



Block Diagram

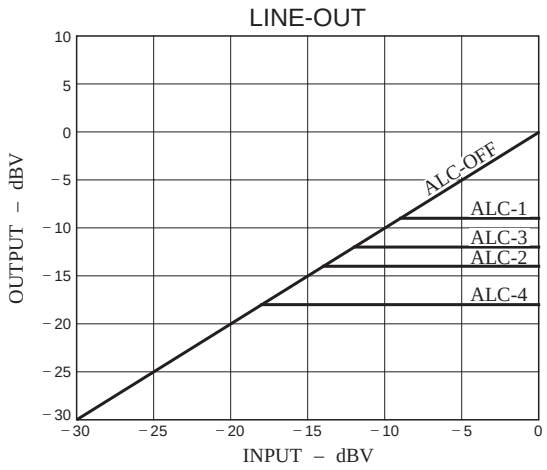


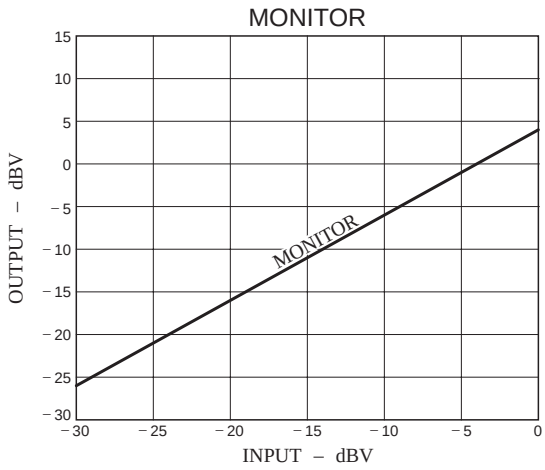
I²C Bit Pattarn

	D8	D7	D6	D5	D4	D3	D2	D1	Condition
*							0	0	AV IN-TV
							0	1	AV IN-1
							1	0	AV IN-2
							1	1	AV IN-3
*						0			Norma
						1			Mute
				0	0				ALC Level-1 (-9dBV)
				0	1				ALC Level-2 (-14dBV)
*				1	0				ALC Level-3 (-12dBV)
				1	1				ALC Level-4 (-18dBV)
*			0						ALC-ON
			1						ALC-OFF
		0							Prohibit
*		1							Fix
*	0								Fix
	1								Prohibit

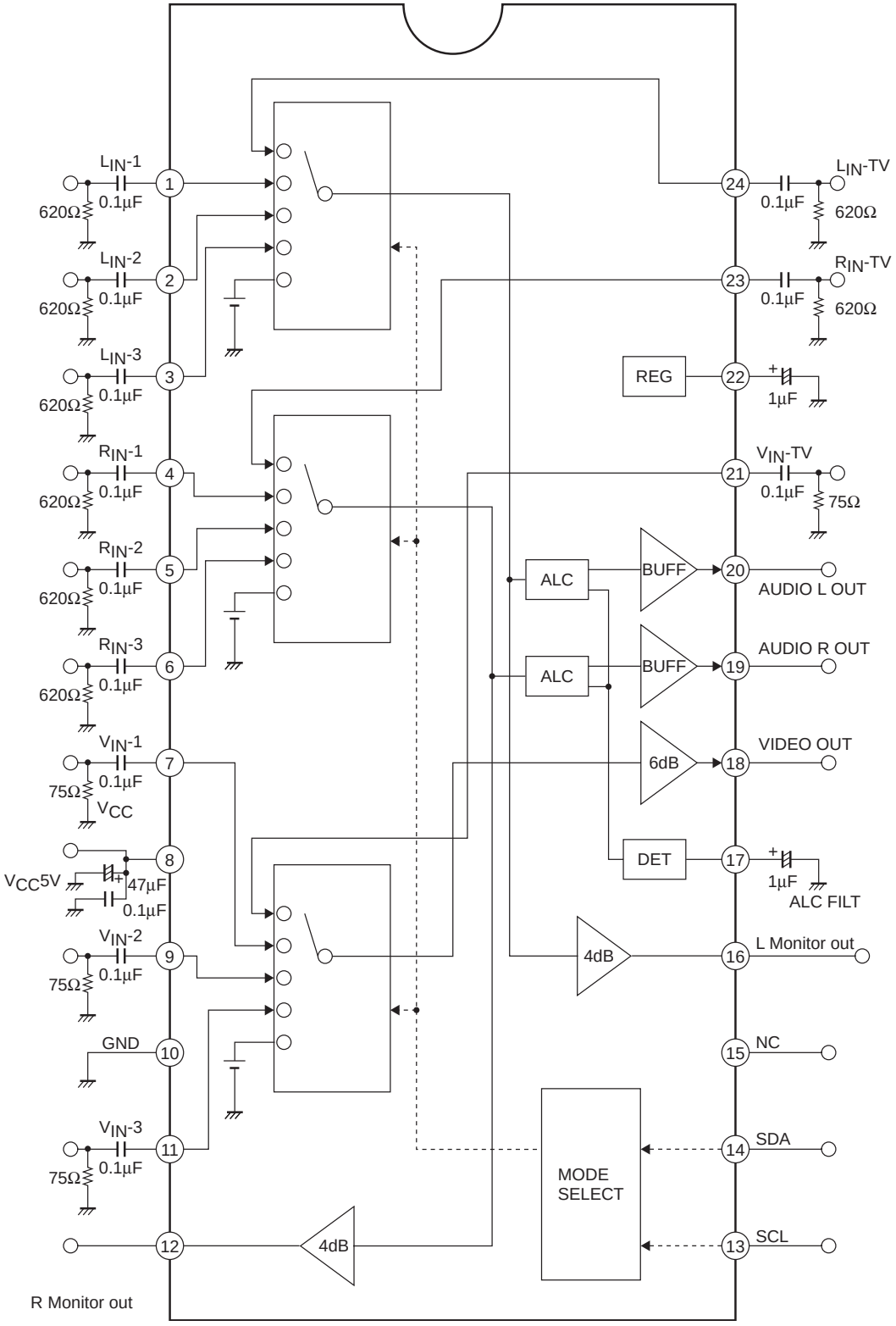
"*" : Shows initial condition.

Slave address : 92h (1001 0010)

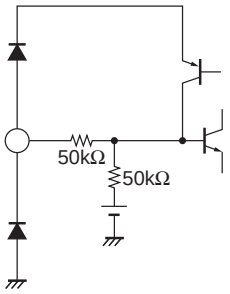
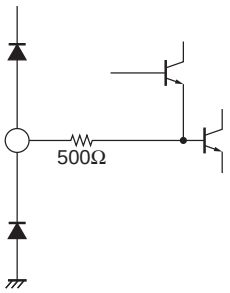
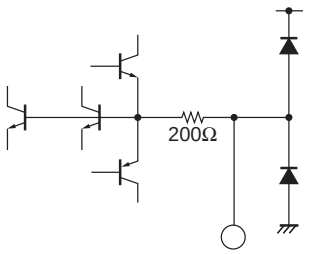
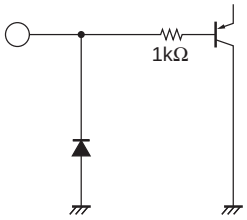
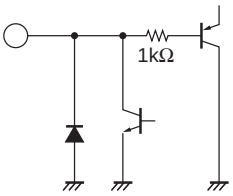
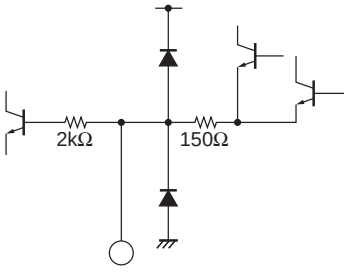




Test Circuit



Pin Functions

Pin No.	Pin Name	Function	DC : voltage AC : level	Equivalent Circuit
1 2 3 4 5 6 23 24	PIA_L1 PIA_L2 PIA_L3 PIA_R1 PIA_R2 PIA_R3 PIA_RTV PIA_LTV	Audio input	DC : 2.4V	
7 9 11 21	PIV_1 PIV_2 PIV_3 PIV_TV	Video input	DC : 1.6V	
8	GND			
10	V_{CC}			
12 16	POMONITR POMONITL	Monitor output	DC : 2.4V	
13	PISCL	Serial clock input		
14	PISDA	Serial data input		
17	POALCFIL	ALC detect filter		

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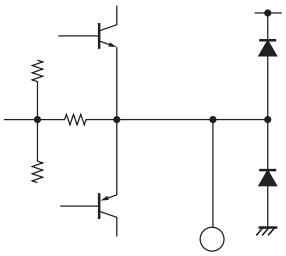
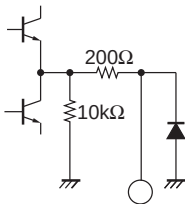
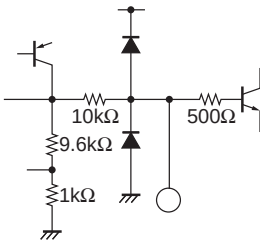
Pin No.	Pin Name	Function	DC : voltage AC : level	Equivalent Circuit
18	POVIDEO	Video output	DC : 1.4V	
19 20	POALCR POALCL	Audio output	DC : 2.4V	
22	PCREG	Reference voltage	DC : 2.4V	

I²C BUS serial interface specification

(1) Data Transfer Manual

This IC adopts control method (I²C-BUS) with serial data, and controlled by two terminals which called SCL (serial clock) and SDA (serial data).At first, set up *1 the condition of starting data transfer, and after that, input 8 bit data to SDA terminal with synchronized SCL terminal clock. The order of transferring is first, MSB (the Most Scale of Bit), and save the order. The 9th bit takes ACK (Acknowledge) period, during SCL terminal takes “H”, this IC pull down the SDA terminal. After transferred the necessary data, two terminals lead to set up and of *2 data transfer stop condition, thus the transfer comes to close.

*1 Defined by SDA fall down SCL during ‘H’ period.
*2 Defined by SDA rise up SCL during ‘H’ period.

(2) Transfer Data Format

After transfer start condition, transfers slave address (92h : 1001 0010) to SDA terminal, control data, then, stop condition (See figure 1).
Slave address is made up of 7bits, *3 8th bit shows the direction of transferring data, but this IC does not have READ mode, so that this bit fix to “L”.
Data works with all of bit, transfer the stop condition before stop 8bit transfer, and to stop transfer, it will be canceled the transfer dates.

*3 It is called R/W bit.

Fig.1 DATA STRUCTURE

START Condition	Slave Address	R/W L	ACK	Control data	ACK	STOP condition

(3) Initialize

This IC is initialized for circuit protection. Initial condition is shown on bitmap.

Reference

Parameter	Symbol	min	max	unit
LOW level input voltage	V_{IL}	-0.5	1.5	V
HIGH level input voltage	V_{IH}	2.5	5.5	V
LOW level output current	I_{OL}		3.0	mA
SCL clock frequency	f_{SCL}	0	100	kHz
Set-up time for a repeated START condition	$t_{SU:STA}$	4.7		µs
Hold time START condition. After this period, the first clock pulse is generated	$t_{HD:STA}$	4.0		µs
LOW period of the SCL clock	t_{LOW}	4.7		µs
Rise time of both SDA and SDL signals	t_R	0	1.0	µs
HIGH period of the SCL clock	t_{HIGH}	4.0		µs
Fall time of both SDA and SDL signals	t_F	0	1.0	µs
Data hold time	$t_{HD:DAT}$	0		µs
Data set-up time	$t_{SU:DAT}$	250		ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0		µs
BUS free time between a STOP and START condition	t_{BUF}	4.7		µs

Definition of timing