



## CURRENT-MODE PWM CONTROLLER

The KA3842A are fixed frequency current-mode PWM controller. They are specially designed for OFF-Line and DC-to-DC converter applications with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totempole output ideally suited for driving a power MOSFET.

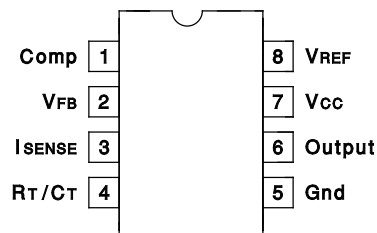
Protection circuitry includes built under-voltage lockout and current limiting.

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The KA3842A, KA384AM can

The KA3842A

have Start-Up Current 0.45 mA



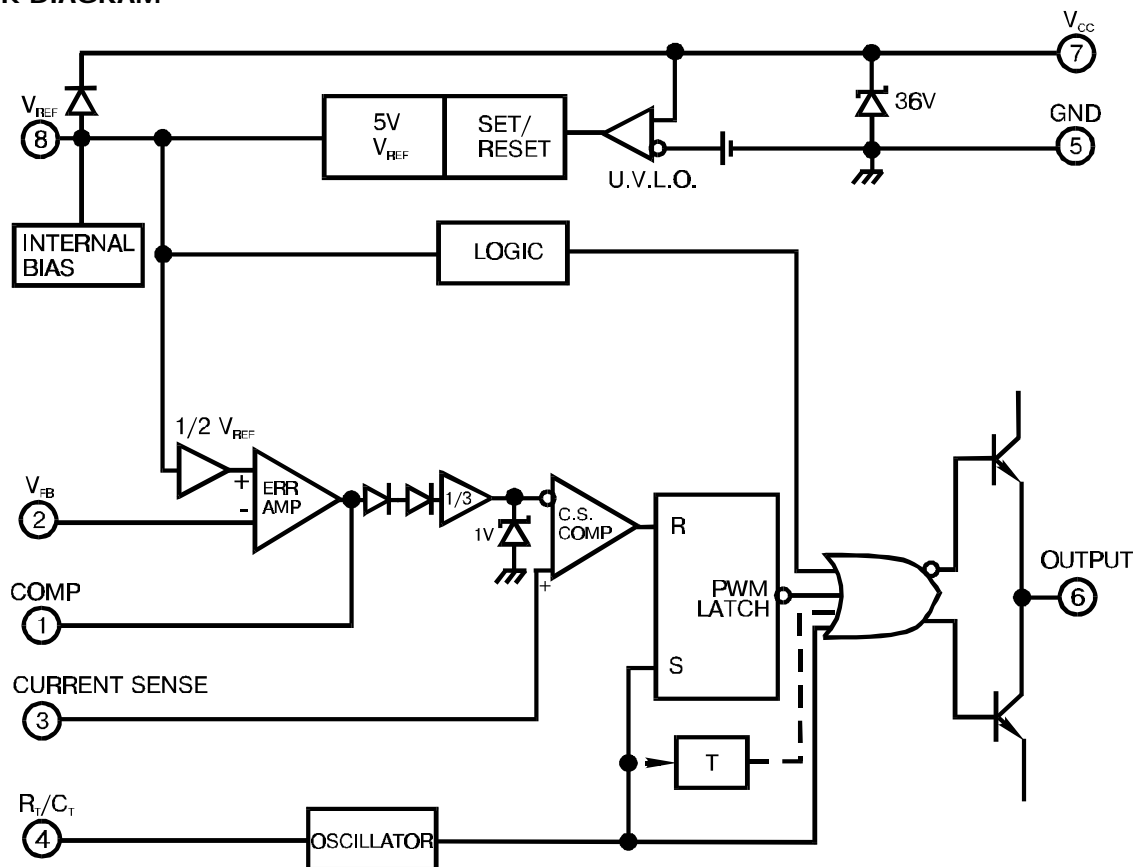
## FEATURES

- Low Start-Up Current
- Maximum Duty Cycle
- U/V Lockout With Hysteresis
- Operating Frequency Up To 500kHz

## ordering information

Device	Package	Operating temperature
KA3842AM	SO-8	0 to +70°C

## BLOCK DIAGRAM



## Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply Voltage	$V_{CC}$	30	V
Output Current	$I_O$	$\pm 1$	A
Analog Inputs	$V_I$	-0.3 to $V_{CC}$	V
Error Amp Output Sink Current	$I_{SINK(E.A)}$	10	mA
Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_O$	1	W



**Electrical characteristics (\*V<sub>CC</sub>=15V, R<sub>T</sub>=10kΩ, C<sub>T</sub>=3.3nF, T<sub>A</sub>=0°C to +70°C, unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Section						
Reference Output Voltage	V <sub>REF</sub>	T <sub>J</sub> = 25°C, I <sub>REF</sub> = 1 mA	4.9	5.0	5.1	V
Line Regulation	ΔV <sub>REF</sub>	12V ≤ V <sub>CC</sub> ≤ 25 V		6.0	20	mV
Load Regulation	ΔV <sub>REF</sub>	1 mA ≤ I <sub>REF</sub> ≤ 20mA		6.0	25	
Short Circuit Output Current	I <sub>SC</sub>	T <sub>A</sub> = 25°C		-100	-180	mA
Oscillator Section						
Oscillation Frequency	f	T <sub>J</sub> = 25°C	47	52	57	KHz
Frequency Change with Voltage	Δf/ΔV <sub>CCF</sub>	12V ≤ V <sub>CC</sub> ≤ 25 V		0.05	1.0	%
Oscillator Amplitude	V <sub>(OSC)</sub>			1.6		V <sub>p-p</sub>
Error Amplifier Section						
Input Bias Current	I <sub>BIAS</sub>			-0.1	-2	μA
Input Voltage	V <sub>I(E.A)</sub>	V <sub>1</sub> = 2.5V	2.42	2.5	2.58	V
Open Loop Voltage Gain	G <sub>VO</sub>	2V ≤ V <sub>O</sub> ≤ 4V	65	90		dB
Power Supply Rejection Ratio	PSRR	12V ≤ V <sub>CC</sub> ≤ 25 V	60	70		
Output Sink Current	I <sub>SINK</sub>	V <sub>2</sub> = 2.7V, V <sub>1</sub> = 1.1V	2	7		mA
Output Source Current	I <sub>SOURCE</sub>	V <sub>2</sub> = 2.3V, V <sub>1</sub> = 5V	-0.5	-1.0		mA
High Output Voltage	V <sub>OH</sub>	V <sub>2</sub> = 2.3V, R <sub>L</sub> = 15KΩ to GND	5.0	6.0		V
Low Output Voltage	V <sub>OL</sub>	V <sub>2</sub> = 2.7V, R <sub>L</sub> = 15KΩ to PIN 8		0.8	1.1	
Current Sense Section						
Gain	G <sub>V</sub>	(Note 1 & 2)	2.85	3.0	3.15	V/V
Maximum Input Signal	V <sub>I(MAX)</sub>	V <sub>1</sub> = 5V (Note1)	0.9	1.0	1.1	V
Power Supply Rejection Ratio	PSRR	12V ≤ V <sub>CC</sub> ≤ 25 V (Note 1)		70		dB
Input Bias Current	I <sub>BIAS</sub>			-3.0	-10	μA
Output Section						
Low Output Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 20 mA		0.08	0.4	V
		I <sub>SINK</sub> = 200 mA		1.4	2.2	
High Output Voltage	V <sub>OH</sub>	I <sub>SINK</sub> = 20 mA	13	13.5		
		I <sub>SINK</sub> = 200 mA	12	13.0		
Rise Time	t <sub>R</sub>	T <sub>J</sub> = 25°C, C <sub>L</sub> = 1nF (Note 3)		45	150	nS
Fall Time	t <sub>F</sub>	T <sub>J</sub> = 25°C, C <sub>L</sub> = 1nF (Note 3)		35	150	
Under-Voltage Lockout Section						
Start Theshold	V <sub>TH(ST)</sub>		14.5	16.0	17.5	V
Min. Operating Voltage (After Turn On)	V <sub>OPR(min)</sub>		8.5	10	11.5	V
PWM Section						
Max. Duty Cycle	D <sub>(MAX)</sub>		95	97	100	%
Min. Duty Cycle	D <sub>(MAX)</sub>				0	
Total Standby Current						
Start-Up Current	I <sub>ST</sub>			0.17	0.3	mA
Operating Supply Current	I <sub>CC (OPR)</sub>	V <sub>3</sub> = V <sub>2</sub> = 0V		14	17	
Zener Voltage	V <sub>Z</sub>		30	38		V

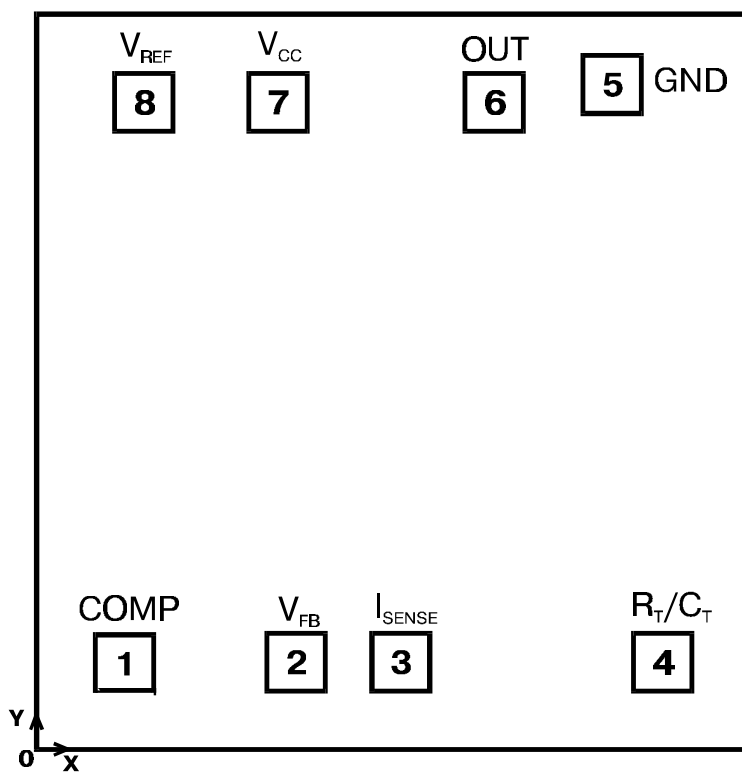
\* Adjust V<sub>CC</sub> above the start threshold before setting at 15V

Note 1: Parameter measured at trip point of lath with V<sub>2</sub>=0

Note 2: Gain defined as A=ΔV<sub>1</sub>/ΔV<sub>3</sub> ; 0 ≤ V<sub>3</sub> ≤ 0.8V

Note 3: These parameters, although guaranteed, are not 100% tested in production.

## Pad Location



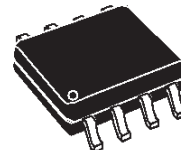
Chip size: 2.38 x 1.63 mm

Pad N	Coordinates μm		Pad N	Coordinates μm	
	X	Y		X	Y
1	90	110	5	1680	1450
2	1050	110	6	1310	1410
3	1310	110			
4	2000	150	7	815	1410
			8	460	1390

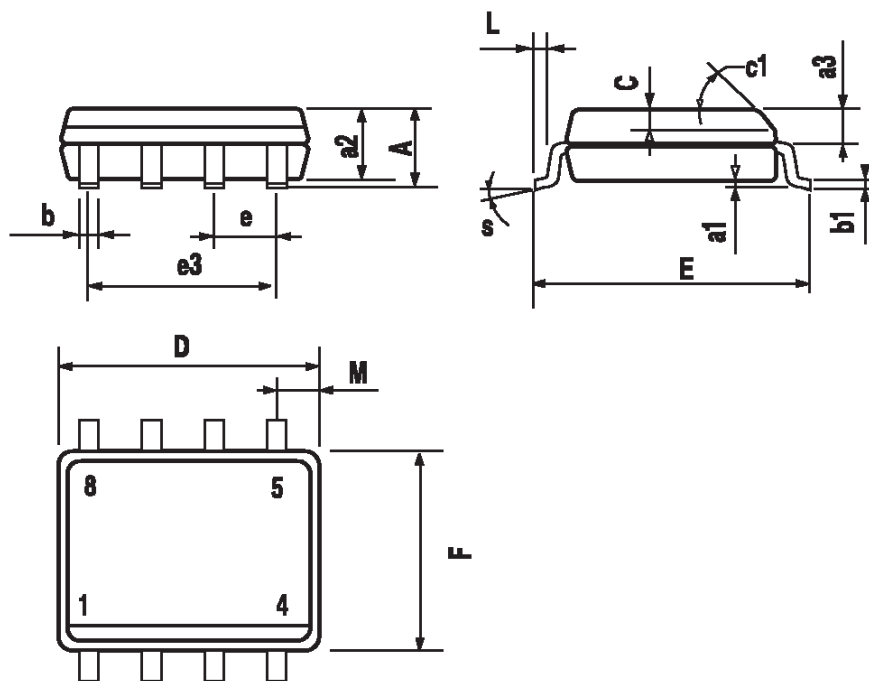
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D (1)	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F (1)	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

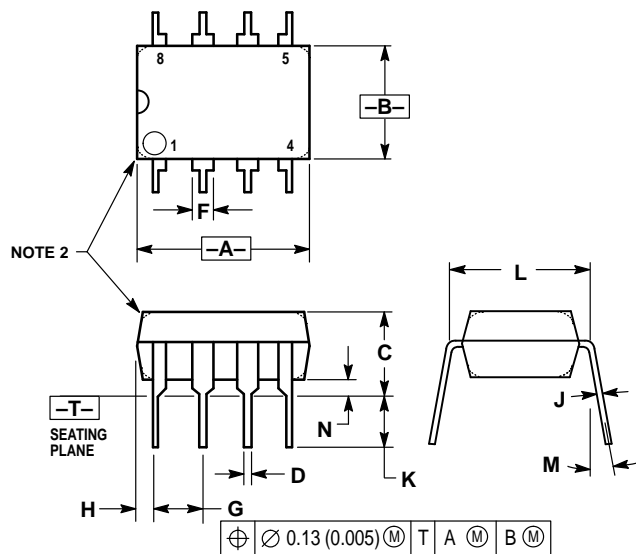
(1) D and F do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006inch).

## OUTLINE AND MECHANICAL DATA



**SO8**





NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	10°		10°	
N	0.76	1.01	0.030	0.040