UM9151

Pulse Dialer

Features

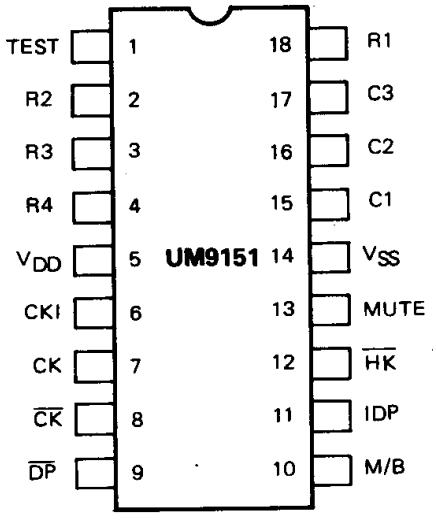
- Direct telephone line operation
- 4 x 3 matrix single contact keyboard
- Supply voltage range 2.5V to 5V
- Inexpensive RC oscillator
- Low power standby mode for redial
- 22 digit capacity for redial
- 18 lead dual-in-line package.
- Redial with either * or # key
- Dialer reset for line power break > 200 msec.
- Pin selectable inter-digital pause (IDP)
- Pin selectable make/break (M/B)
- High speed test capability

General Description

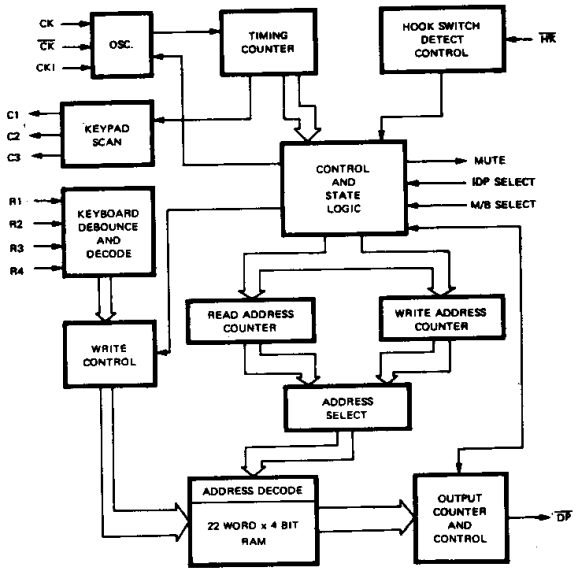
The UM9151 pulse dialer is a monolithic CMOS integrated circuit which converts pushbutton inputs to a series of pulses suitable for telephone dialing. It is intended to replace mechanical telephone dialers and can operate directly from the telephone lines. The pulse dialer function is implemented using two outputs; one pulses the line; the other mutes the receiver.

CMOS technology used to produce this device results in very low power consumption and enables easy interfacing with a variety of telephones with high noise immunity and few external components.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

DC Supply Voltage . . . . . –0.3V to 6V

Operating Temperature . . . . . –20°C to 60°C

Storage Temperature . . . . . –55°C to 125°C

*Comments

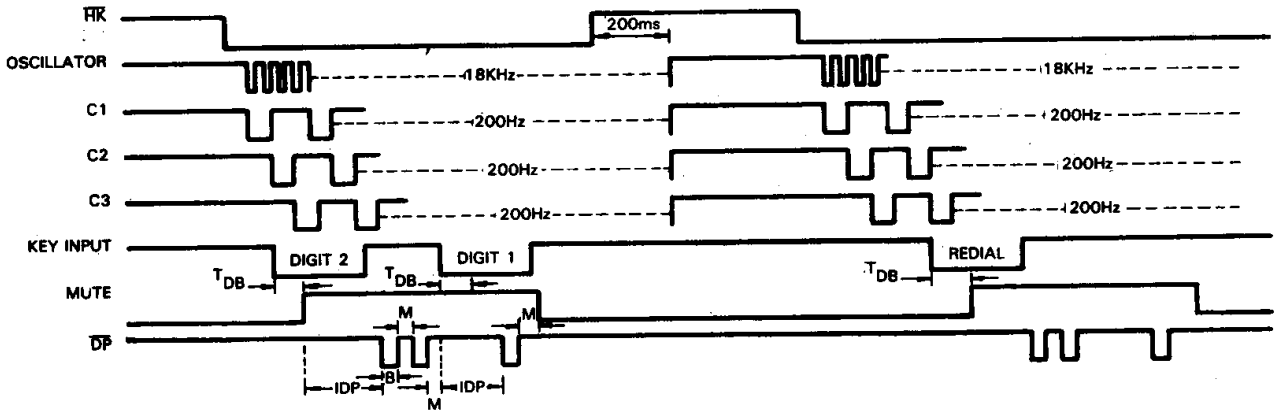
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(V_{SS} = 0V, V_{DD} = 3.5V, T_{op} = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{DD}	DC Supply Voltage	2.5	–	5	V	–
	Supply Current					
I_S	Standby	–	–	1	μA	V_{DD} = 2.5V With pins 1, 10, and 11 connected.
I_D	Operating	–	–	150	μA	V_{DD} = 5V Pin 9 is open.
	Keyboard Contact					
R	Resistance	–	–	1	KΩ	–
C	Capacitance	–	–	30	pF	–
T_{DB}	Key Input Debounce Time	6.7	–	–	ms	–
I_{MS}	Mask Sink Current	500	–	–	μA	V_{DD} = 2.5V V_O = 0.5V
I_{MD}	Mask Driving Current	500	–	–	μA	V_{DD} = 2.5V V_O = 2V
I_{LS}	Line Sink Current	500	–	–	μA	V_{DD} = 2.5V V_O = 0.5V
I_{LL}	Line Leakage Current	–	–	1	μA	V_{DD} = 5V V_O = 5V
I_{TD}	Tone Driving Current	250	–	–	μA	V_{DD} = 2.5V V_O = 2V
F_{OSC}	Oscillation Frequency	–	18	–	KHz	Per typical application, V_{DD} = 3.5V
ΔF/F	Frequency Variation vs Voltage	0	–	+4	%	V_{DD} = 2.5 ~ 3.5V, $(F_{3.5}-F_{2.5})/F_{3.5}$
ΔF/F		0	–	+4	%	V_{DD} = 3.5 ~ 5V, $(F_5-F_{3.5})/F_5$
ΔF/F	Frequency Variation per Lot	–4	–	+4	%	Per typical application V_{DD} = 3.5V
T_{IDP}	Inter-digital Pause	–	500 800	– –	ms ms	F_{OSC} = 18KHz.

Timing Diagram



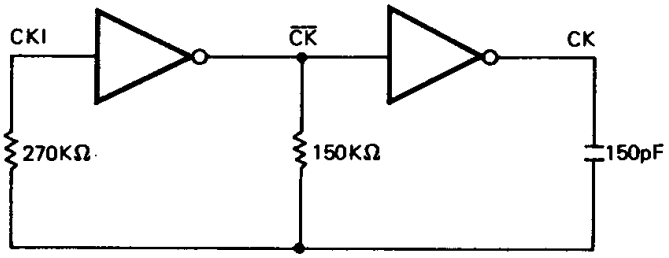
Pin Description

Pin	Consignation	Description
1	TEST	Dialing rate = 10pps when connected to V_{DD}. (normal) Dialing rate = 600pps when connected to V_{SS}. (high speed test)
18, 2, 3, 4	R_1, R_2, R_3, R_4	Keyboard inputs.
5	V_{DD}	Positive power supply.
6, 7, 8	CKI, CK, $\overline{CK}$	These pins are connected to an RC oscillator. (clock frequency control)
9	$\overline{DP}$	Dialing pulse output. The output stage is an N-channel open drain device.
10	M/B	M/B = 33⅓/66⅔ if connected to V_{DD}. M/B = 40/60 if connected to V_{SS}.
11	IDP	IDP = 500ms if connected to V_{DD}. IDP = 800ms if connected to V_{SS}.
12	$\overline{HK}$	On-hook/Off-hook input.
13	MUTE	MUTE out to mute telephone speech circuit.
14	V_{SS}	Negative power supply.
15, 16, 17	C_1, C_2, C_3	Keyboard outputs.

Functional Description

Oscillator

The oscillator consists of two inverters and external components which control the oscillation frequency. The circuit is sufficiently versatile to allow a variety of component combinations. The oscillation circuit detailed below, has an oscillation frequency of 18KHz for 10 pps dialing rate.



oscillator circuit

4 x 3 Matrix Mode

A pulse to logic low is sequentially switched around the three keyboard scan outputs and requires 5 ms for a complete scan cycle. When a key is depressed, the pulse (logic low) appears on one of the four keyboard inputs (provided with on-chip pull up resistors to logic high). Following key depression and 6.7 ms antibounce period, the data is entered to RAM. Before a second key depression can be recognized, the first key must be released and a full antibounce period completed without a pulse appearing on any input. If two or more keys are depressed during the same scan cycle, the data will be rejected and another full antibounce period must be completed without a pulse appearing on any of the inputs before the next key depression is recognized.

$\overline{HK}$

External circuitry connected to $\overline{HK}$ input is used to indicate whether the telephone handset is on-hook or off-hook, these two states being represented by logic HIGH, logic LOW respectively. If power is present on the dialer, this input should normally be held at logic LOW. If the $\overline{HK}$ input is taken to logic HIGH for a period of less than 200 msec and then returned to logic LOW, no action is taken and the dialer will continue to function.

If it is taken to logic HIGH for a period greater than 200 msec., oscillator and any dialing sequence will cease. All internal counters will be reset, though the contents of the RAM will be unaffected. Taking the input back to logic LOW will restart the keyboard scan and dialing sequence and the dialer will wait for a data entry.

$\overline{DP}$

The loop-disconnect dial pulses appear at the $\overline{DP}$ output. The output stage consists of an N-channel open drain device sinking current to V_{SS}. During a dial pulse break period the output device is switched on and during the make period and IDP the output device is switched off. The output drives an external bipolar transistor that sequentially opens the telephone loop a number of times equal to the input digit selected. For example, key 7 will generate 7 loop current breaks.

MUTE

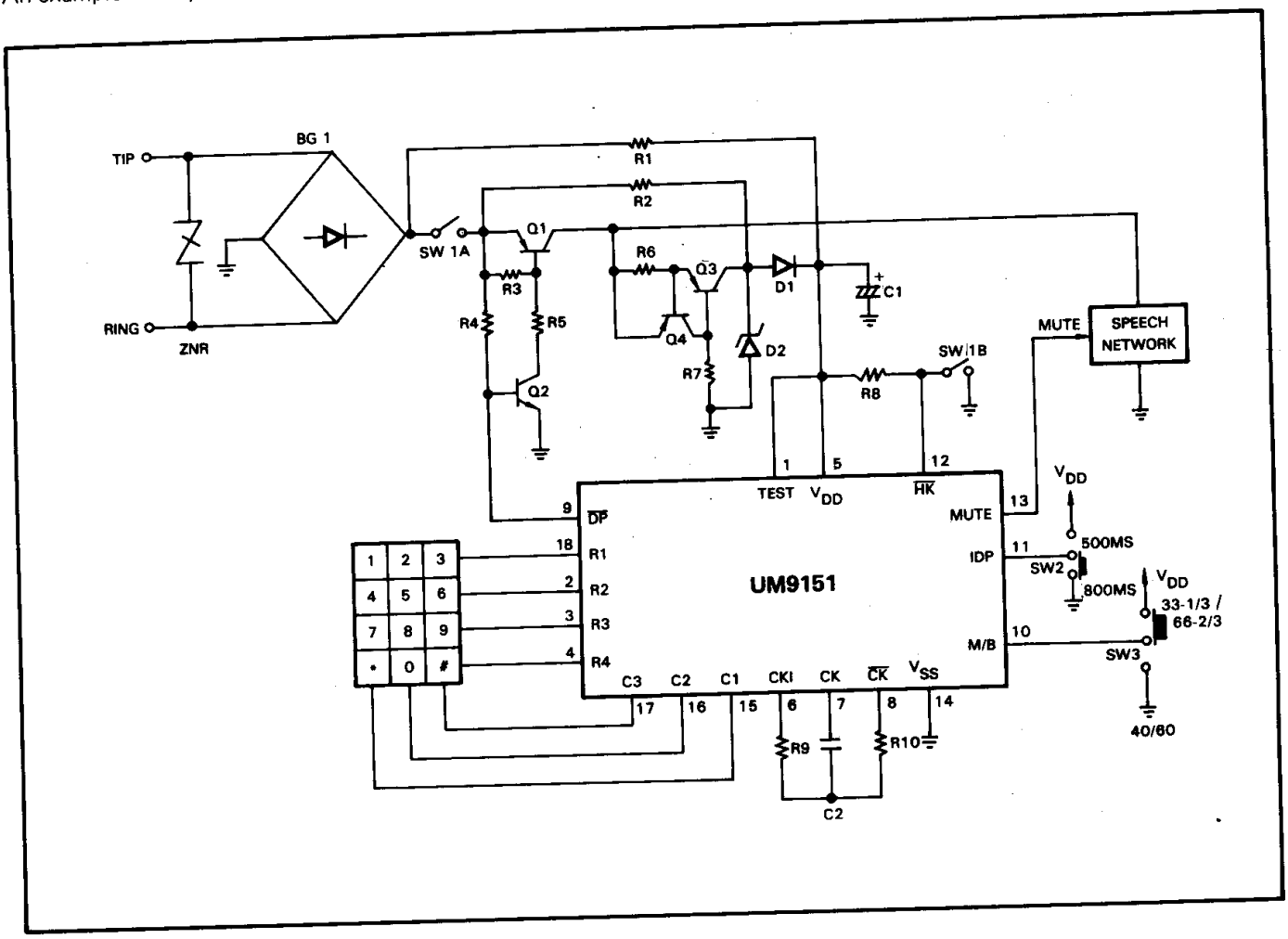
The MUTE output is used to control the muting of the telephone network during out dialing. A logic HIGH indicates that the telephone is to be muted, the transition to logic HIGH occuring immediately on recognition of a key depression.

Redialing

The keyboard inputs are accepted at an asynchronous rate, load into a first-in-first-out RAM. If the call is not successful, it can be redialed at a later time by pressing the redial key * or #, and the correct number of pulses begins to read out. For example, dialing 0 1 2 3 4 5 6 and on-hook a period of valid redialing, when off-hook again, pressing the redial key * or #, RAM will read out 0 1 2 3 4 5 6. Since UM9151 allows only one key to be entered before pressing the redial key, it is suitable for use in a PABX system. For example, dialing 0 1 2 3 4 5 6 and on-hook a period of valid redialing, when off-hook again, pressing any key "N" (N = 0, 1, 2, . . . , 9) except * or #, then pressing the redial key, RAM will read out 1 2 3 4 5 6.

Typical Application

An example of loop disconnect UM9151 interface



Circuit Description

1. **Loop Disconnect Interface:** Q_1, Q_2, R_3, R_4, R_5 and $\overline{DP}$

   Q_1 and Q_2 act as switching transistors, $\overline{DP}$ is the dial pulse output which drives Q_2 transistor on and off as make and break, R_4 pulls up the $\overline{DP}$ output, R_3 protects the Q_1 transistor during break period and R_5 limits the base current of Q_1.

2. **Power supply:** R_1, R_2, R_6, R_7, Q_3, Q_4, D_1, D_2 and C_1

   A current source is constructed by R_6, R_7, Q_3 and Q_4. It can supply a 600 μA constant current to UM9151 which is indpendent from the line power variation. D_2 can protect this chip under 5.6V. R_2, the power intial loop, supplies the intial power at off-hook instant. R_1, the data retention loop, retains the memory during on-hook.

3. **Oscillator:** $\overline{CKI}$, $\overline{CK}$, CK, R_9, R_{10} and C_2

   The oscillation frequency is 18 KHz for 10 pps dialing.

Parts List

BG1: IN4001x4
Q_1: 2N5401
Q_2: 2N5551
Q_3: 2N5401
Q_4: 2N5401
R_1: 22M
R_2: 220K
R_3: 220K
R_4: 220K
R_5: 3K3
R_6: 1K
R_7: 100K
R_8: 220K
R_9: 270K
R_{10}: 150K
C_1: 47μF/10WV
C_2: 150pF
D_1: 1N4148
D_2: 5V6/0.5W ZD