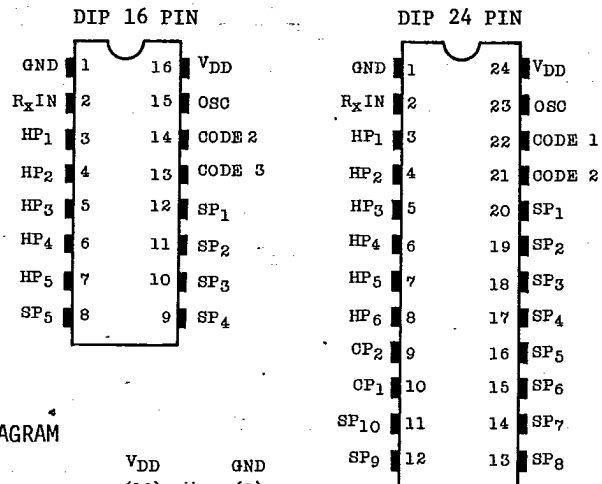




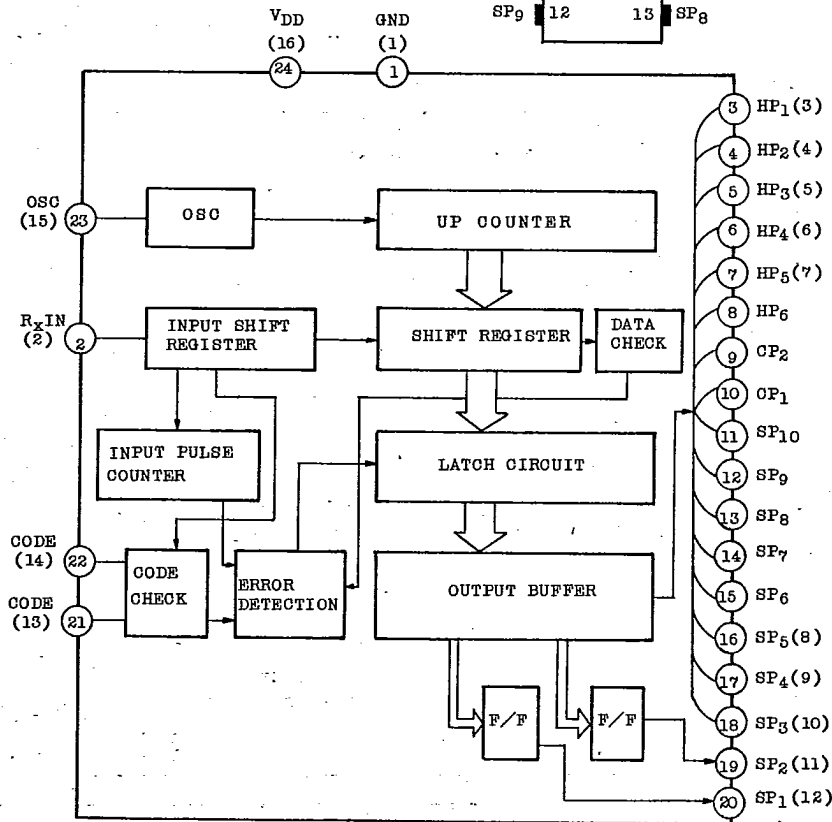
# TC9149P, TC9150P

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## PIN CONNECTIONS



## BLOCK DIAGRAM



PIN NO. OF TC9149P  
IS GIVEN IN  
PARENTHESIS.

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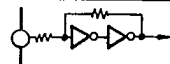
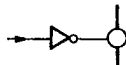
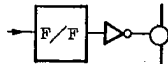
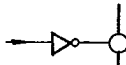
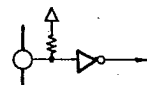
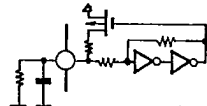
# TC9149P, TC9150P

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## ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=25°C, VDD=5V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	VDD	-	Ta=-20~75°C	4.5	~	5.5	V
Operating Supply Current	IDD	-	Output without Load	-	-	1.0	mA
Oscillation Frequency	fOSC	-	Ta=-20~75°C, VDD=4.5~5.5V	27	~	57	kHz
Standard OSC Frequency	SfOSC	-		-	38	-	kHz
Variance of Oscillation Frequency by VDD	$\Delta V_{fOSC}$	-	Ta=25°C, VDD=4.5~5.5V	-5	-	5	%
Variance of Oscillation Frequency by Temperature	$\Delta T_{fOSC}$	-	Ta=-30~75°C	-5	-	5	%
Output Current	"H" Level	IOH	all output, VOH=4V	-	-	-1.0	mA
	"L" Level	IOL	all output, VOL=1V	1.0	-	-	mA
Input Current	"H" Level	IIH	CODE Terminal, VIH=5.0V	-1.0	-	1.0	μA
Pull-up Resistor	Rup	-	CODE Terminal	10	20	40	kΩ
Input Circuit Threshold Voltage	VIN	-	Rx Terminal	2.0	2.5	3.0	V
Hysteresis Width	VHIS	-	Rx Terminal	~	0.8	-	V

## DESCRIPTION OF TERMINALS

PIN NO.		SYMBOL	TERMINAL	FUNCTION/OPERATION	INPUT/OUTPUT-CONFIGURATION
16 PIN	24 PIN				
1	1	GND	GND		
2	2	R <sub>x</sub> IN	Receiving signal Input	Instruction signal with carrier signal eliminated is input.	
3~7	-	HP1~HP5	Continuous signal Input	As long as receiving signal is input, this output is held at "H" level.	
-	3~8	HP1~HP6			
-	9~10	CP1~CP2	Cyclic signal output	When receiving signal is input, output is reversed.	
8~12	-	SP1~SP5	Single-shot signal output	When receiving signal is input, output is placed at "H" level only for a fixed time. (about 107 msec)	
-	11~20	SP1~SP10			
13~14	21~22	CODE	Code input	Transmitter code is compared with a code set at this terminal and if they agree each other, input is accepted.	 Built-in pull-up resistor
15	23	OSC	Timing oscillation	A resistor and a capacitor are parallelly connected between this terminal and GND.	
16	24	VDD	Power Supply		

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# TC9149P, TC9150P

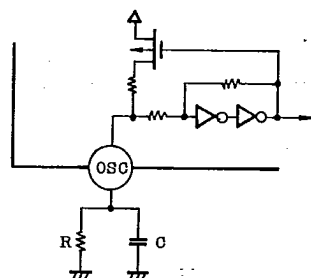
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## FUNCTIONAL DESCRIPTION

### 1. OSCILLATION CIRCUIT

Timing with transmitter signal and internal operating clock are all decided by this oscillator.

The oscillator has been so far constructed through a combination of a linear amplifier by means of C MOS inverter in IC and 455 kHz ceramic resonator; however, when TC9149P/TC9150P is used, a stable oscillator can be constructed by parallelly connecting C and R between the oscillator and GND by a single terminal oscillator.



$R : 39k\Omega \pm 5\%$

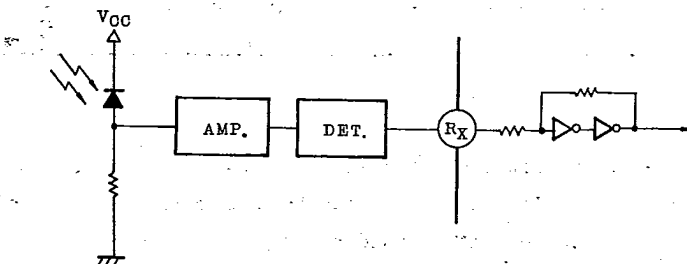
$C : 1000pF \pm 5\%$

(POLYPROPYLENE FILM CAPACITOR SHOULD BE USED.)

Oscillation frequency is about  $38\text{ kHz} \pm 5\text{ kHz}$  at  $R=39k\Omega$  and  $C=1000pF$ .  
(Refer to Graph 1 Oscillation Frequency Characteristic)

### 2. RECEIVING SIGNAL INPUT CIRCUIT

Signal received by the light receiving element is sent through the amplifier to the detector where 38 kHz carrier wave is eliminated and is input into the receiving signal input circuit. The receiving signal input circuit (Rx IN) has a built-in Schmitt circuit for shaping receiving signal waveform to eliminate rounding.



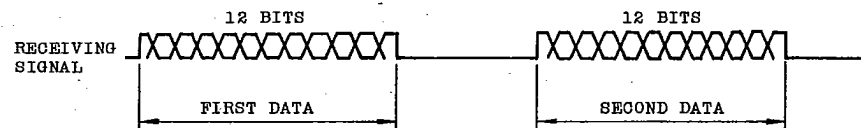
AUDIO DIGITAL IC

# TC9149P, TC9150P

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## 3. RECEIVING SIGNAL CHECK

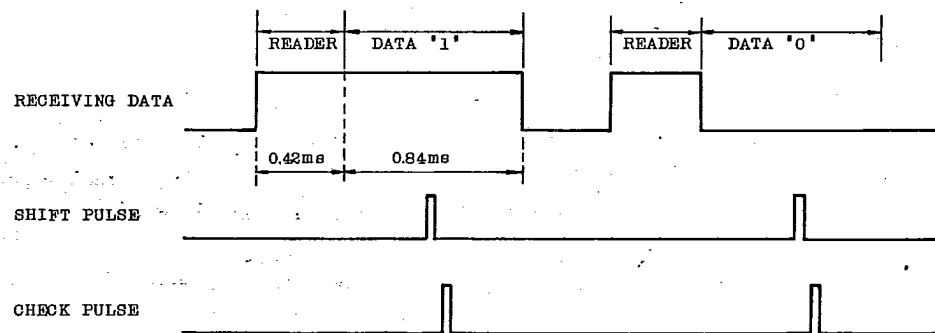
The receiving signal check is to check 2 cycle transmitting signal sent from the transmitter to determine if it is normal signal.



First, the first data is stored in the 12-bits shift register. Then, when the second data is put into the shift register, data is forced out of the shift register by one bit, where the first data has been stored.

Now, pushed out data and incoming data are checked to see if they are same.

If an error is caused in the receiving data 12-bits check, the system is reset at that point of time. Conversely, when all receiving data are OK, output is raised from "L" level to "H" level.



The status of receiving data, shift pulse and check pulse is shown above.

Shift pulse is provided in the data center by taking frequency margins of the transmitter and the receiver into consideration.

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# TC9149P, TC9150P

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## Code Comparison

To prevent interference with other models, C1, C2 and C3 code bits are provided for checking whether the transmitter and receiver codes agree each other.

Only when both codes agreed, internal latch strobe pulse is generated to latch receiving data and output is raised from "L" level to "H" level. If both codes do not agree, no latch strobe pulse is generated and output remains at "L" level.

Code bits used differ depending upon receiver as shown below:

CODE BIT	
C <sub>1</sub>	C <sub>2</sub>
C <sub>3</sub>	C <sub>2</sub>
1	0
0	1
1	1

TC9149P .... C2, C3 CODE BIT

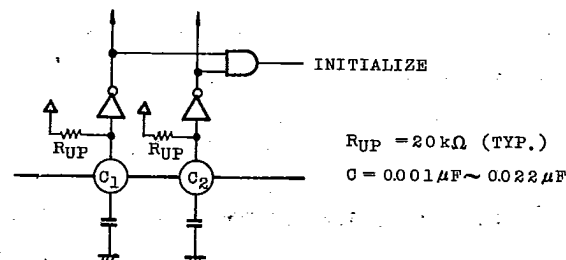
TC9150P .... C1, C2 CODE BIT

\* CODE BIT '0', '0' CANNOT BE USED.

## 4. INITIALIZATION AT TIME OF POWER ON

In order to initialize the internal status at time of power ON, it is necessary to perform the initialization.

The initialization is carried out when a capacitor is connected to the code bit terminal.



- \* In case of TC9149P, connect a capacitor to C2 and C3.
- \* A capacitor for initialization is unnecessary for the terminal for which Code Bit "0" is selected. However, Code Bit "0", "0" cannot be used. Either one terminal must be set at "H".

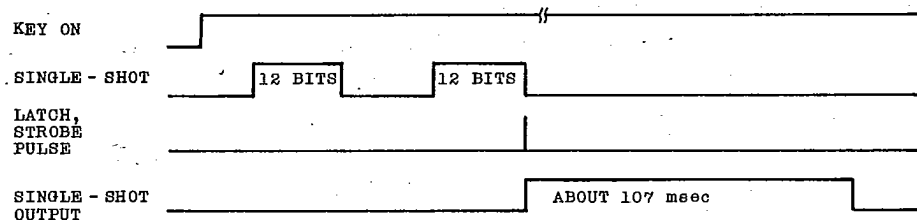
AUDIO DIGITAL IC

# TC9149P, TC9150P

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## 5. EXPLANATION OF OUTPUT PULSE SP, HP, CP

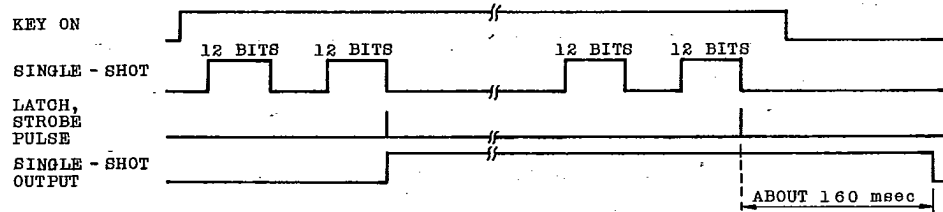
### 5-1. SP1 - SP10 (Single pulse)



After checking 12-bits receiving data, if data agree and OK, single pulse is output.

Output is raised from "L" level to "H" level and returned again to "L" level after about 107 msec.

### 5-2. HP1 - HP6 (Hold pulse)



Hold pulse is output by the first latch strobe pulse after key ON.

Output is kept at "H" level as long as Continuous Signal is input.

When the key is released and continuous signal is stopped, about 160 msec later, output is reversed to "L" level by the last latch strobe pulse.

Further, HP1 - HP6 are able to parallelly and simultaneously max sextet outputs at "H" level by continuous signal sent from the transmitter.

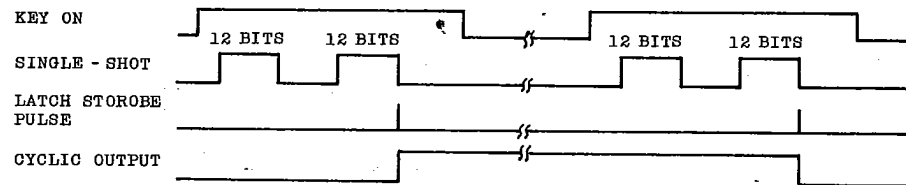
These outputs are optimum as outputs of REC-PALY, REC-PAUSE, and CUE/REVIEW of a tape deck.

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# TC9149P, TC9150P

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## 5-3. CP1, CP2 (Cyclic pulse)



When single-shot signal is received, cyclic pulse output is reversed.  
This cyclic pulse is used for power ON/OFF, MUTE, etc.

## 6. CODE ALLOCATION (KEY No. is of TC9148P)

KEY №	DATA BIT										FUNCTION OF INSTRUCTION	
	H	S <sub>1</sub>	S <sub>2</sub>	K <sub>1</sub>	K <sub>2</sub>	K <sub>3</sub>	K <sub>4</sub>	K <sub>5</sub>	K <sub>6</sub>			
1	1	0	0	1	0	0	0	0	0	0	CONTINUOUS SIGNAL	HP <sub>1</sub>
2	1	0	0	0	1	0	0	0	0	0	"	HP <sub>2</sub>
3	1	0	0	0	0	1	0	0	0	0	"	HP <sub>3</sub>
4	1	0	0	0	0	0	1	0	0	0	"	HP <sub>4</sub>
5	1	0	0	0	0	0	0	1	0	0	"	HP <sub>5</sub>
6	1	0	0	0	0	0	0	0	1	0	"	HP <sub>6</sub>
7	0	1	0	1	0	0	0	0	0	0	SINGLESHOT SIGNAL	SP <sub>1</sub>
8	0	1	0	0	1	0	0	0	0	0	"	SP <sub>2</sub>
9	0	1	0	0	0	1	0	0	0	0	"	SP <sub>3</sub>
10	0	1	0	0	0	0	1	0	0	0	"	SP <sub>4</sub>
11	0	1	0	0	0	0	0	1	0	0	"	SP <sub>5</sub>
12	0	1	0	0	0	0	0	0	1	0	"	SP <sub>6</sub>
13	0	0	1	1	0	0	0	0	0	0	"	SP <sub>7</sub>
14	0	0	1	0	1	0	0	0	0	0	"	SP <sub>8</sub>
15	0	0	1	0	0	1	0	0	0	0	"	SP <sub>9</sub>
16	0	0	1	0	0	0	1	0	0	0	"	SP <sub>10</sub>
17	0	0	1	0	0	0	0	1	0	0	CYCLIC SIGNAL	CP <sub>1</sub>
18	0	0	1	0	0	0	0	0	1	0	"	CP <sub>2</sub>

C1 - C3 code bits are available in addition to the above data bits for optional code selection.

TC9150P can use all keys, but TC9149P is able to use KEY1~5 and KEY7~11 only for 10 commands.

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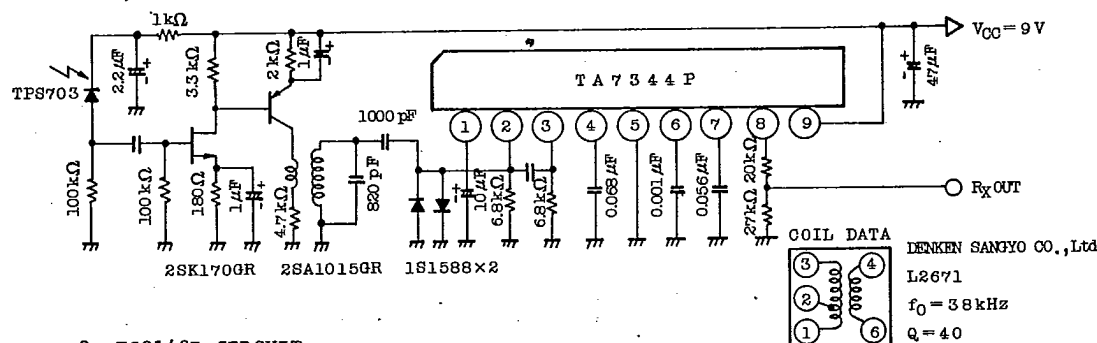
# TOSHIBA, ELECTRONIC 02 DE 9097247 0018053 4

## TC9149P, TC9150P

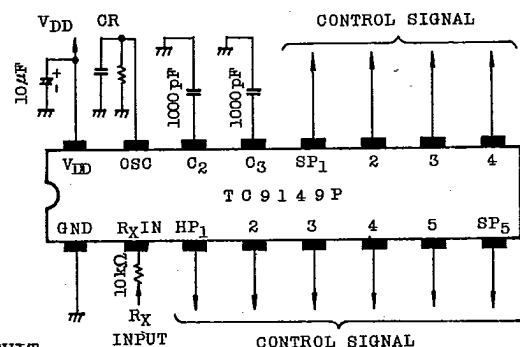
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### 7. APPLICATION CIRCUITS

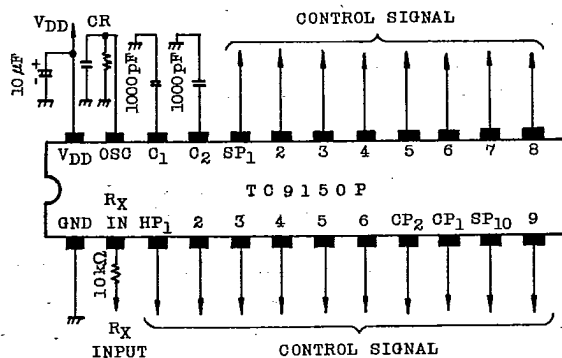
#### 1. RECEIVING SECTION



#### 2. TC9149P CIRCUIT



#### 3. TC9150P CIRCUIT



- \* R should be  $38 \text{ k}\Omega \pm 5\%$ .
- \* C should be polypropylene film capacitor having good temperature characteristics  $1000 \text{ pF} \pm 5\%$ .

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# TC9149P, TC9150P

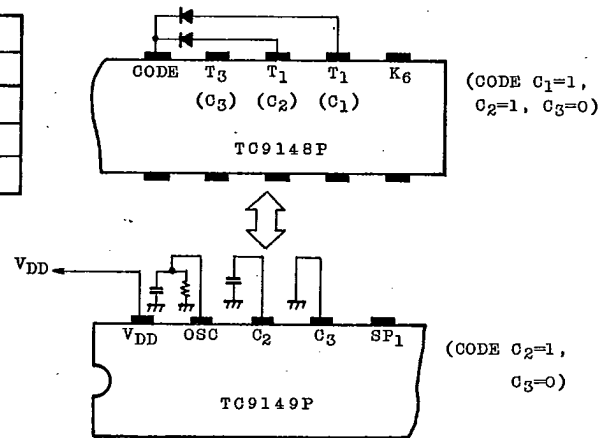
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## NOTE FOR APPLICATION CIRCUIT

### 1. COMBINATION OF TC9148P/TC9149P CODE BITS.

(TABLE 1)

TC9148P			TC9149P	
C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>3</sub>
1	1	0	1	0
1	0	1	0	1
1	1	1	1	1

(EXAMPLE 1) IN CASE CODE C<sub>2</sub>=1 AND C<sub>3</sub>=0

The combination of code bits of TC9148P and TC9149P is shown in Table 1.

To make Code Bit to "1" on TC9148P, connect diodes to CODE terminal from T<sub>1</sub> ~ T<sub>3</sub> Terminals. To set Code Bit at "0", open the circuit.

TC9149P has C<sub>2</sub> and C<sub>3</sub> code terminals. Code bit of C<sub>1</sub> has been pulled up in IC and C<sub>1</sub> is always kept at "1" status.

Therefore, on Transmitter TC9148P it is necessary to keep C<sub>1</sub> code bit at "1".

Example 1 is the external circuit diagram when Code Bit C<sub>2</sub>=1, and C<sub>3</sub>=0.

### 2. COMBINATION OF TC9148P/50P CODE BITS

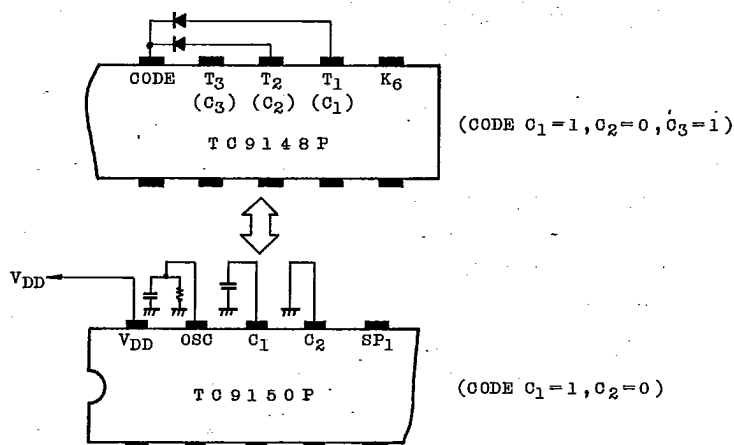
(TABLE 2)

TC9148P			TC9150P	
C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	C <sub>1</sub>	C <sub>2</sub>
1	0	1	1	0
0	1	1	0	1
1	1	1	1	1

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# TC9149P, TC9150P

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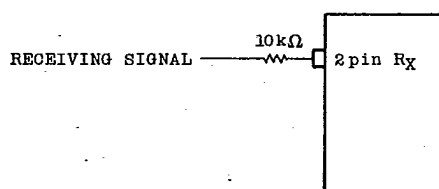
(EXAMPLE 2) IN CASE CODE  $C_1=1$  and  $C_2=0$ 

The combination of Code Bits of TC9148P and TC9150P is shown in Table 2

On TC9150P, C3 code has been pulled up in IC and always kept at "1" status. Therefore, it is necessary to keep Code Bit C3 of Transmitter TC9148P at "1". To keep Code Bit C3 at "1", connect a diode to CODE Terminal from T3 Terminal.

Example 2 is an example of the circuit when Code Bit  $C_1=1$  and  $C_2=0$ .

3. If input voltage above  $V_{DD} + 0.3V$  may possibly be applied to Rx Input Terminal (2 PIN), connect resistors of about  $10k\Omega$  in series to Rx Input Terminal. (This is to prevent latch-up.)

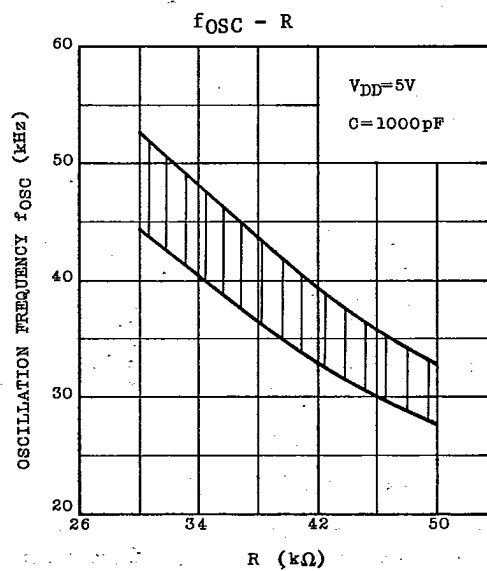
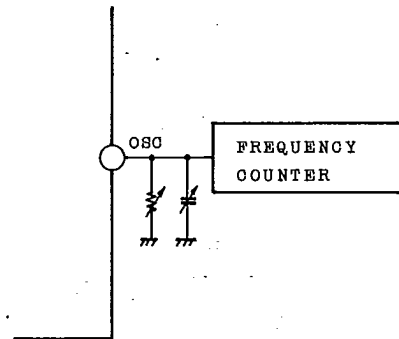
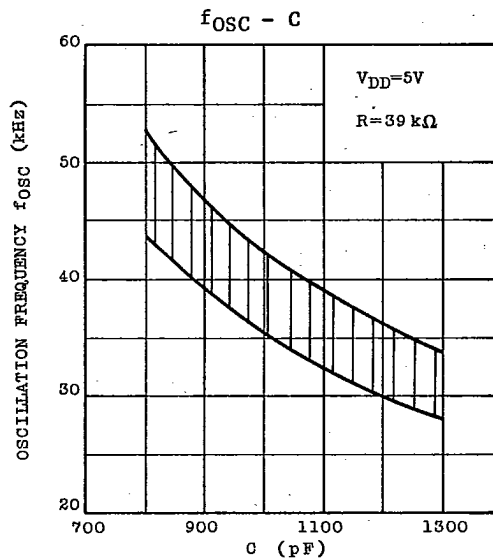


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# TC9149P, TC9150P

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## OSCILLATION FREQUENCY CHARACTERISTICS



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