

### Features

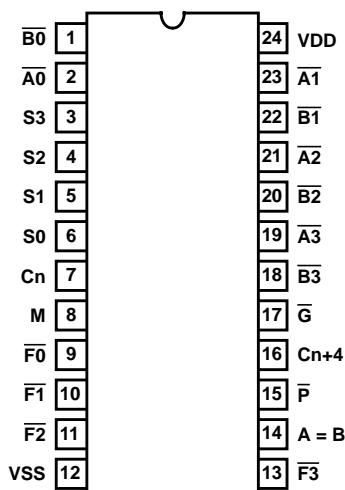
- High Voltage Type (20V Rating)
- Full Look Ahead Carry for Speed Operations on Long Words
- Generates 16 Logic Functions of Two Boolean Variables
- Generates 16 Arithmetic Functions of Two 4 Bit Binary Words
- A = B comparator Output Available
- Ripple Carry Input and Output Available
- Typical Addition Time 200ns at VDD = 10V
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1 $\mu$ A at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Standardized Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications

- Parallel Arithmetic Units
- Process Controllers
- Low Power Minicomputers

### Pinout

CD40181BMS ACTIVE-LOW DATA  
TOP VIEW



### Description

The CD40181BMS is a low power four bit parallel arithmetic logic unit (ALU) capable of providing 16 binary arithmetic operations on two four-bit words and 16 logical functions of two Boolean variables. The mode control input M selects logical (M = High) or arithmetic (M = Low) operation. The four select inputs (S0, S1, S2, and S3) select the desired logical or arithmetic functions, which include AND, OR, NAND, NOR and exclusive-OR and-NOR in the logic mode, and addition, subtraction, decrement, left-shift and straight transfer in the arithmetic mode, according to the truth table. The CD40181BMS operation may be interpreted with either active-low or active-high data at the A and B word inputs and the function outputs F, by using the appropriate truth table.

The CD40181BMS contains logic for full look ahead carry operation for fast carry generation using the carry-generate and carry-propagate outputs  $\bar{G}$  and  $\bar{P}$  for the four bits of the CD40181BMS. Use of the CD40181BMS look-ahead carry generator in conjunction with multiple CD40181BMS's permits high speed arithmetic operations on long words. A ripple carry output Cn+4 is available for use in systems where speed is not of primary importance.

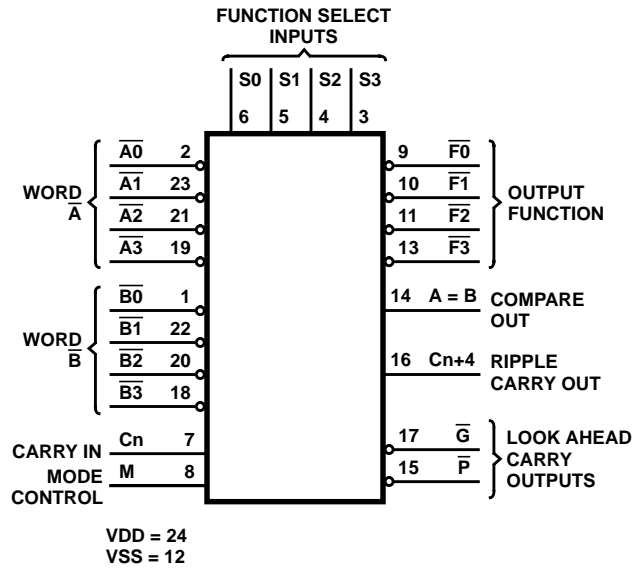
Also included in the CD40181BMS is a comparator output A = B, which assumes a high level whenever the two four-bit input words A and B are equal and the device is in the subtract mode. In addition, relative magnitude information may be derived from the carry-in input Cn and ripple carry-out output Cn+4 by placing the unit in the subtract mode and externally decoding using the information in Table B.

The CD40181BMS is similar to industry types MC14581 and 74181.

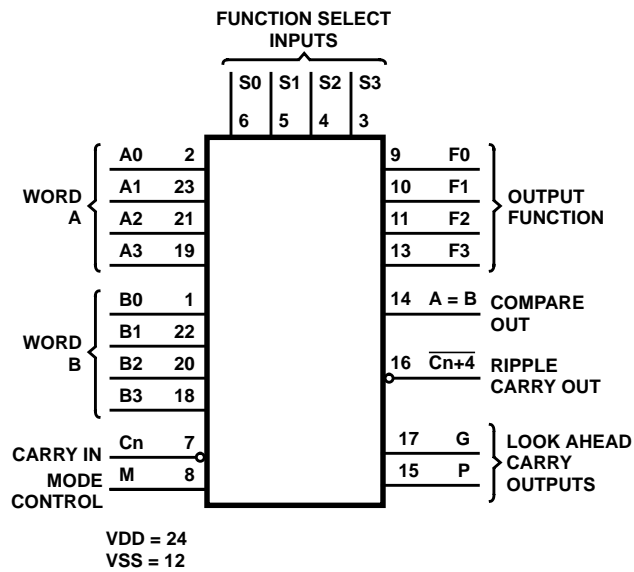
The CD40181BMS is supplied in these 24-lead outline packages:

Braze Seal DIP	HNZ
Ceramic Flatpack	H4P

# Functional Diagrams



ACTIVE-LOW DATA



ACTIVE-HIGH DATA

# Specifications CD40181BMS

## Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V  
(Voltage Referenced to VSS Terminals)  
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V  
DC Input Current, Any One Input . . . . . ±10mA  
Operating Temperature Range . . . . . -55°C to +125°C  
Package Types D, F, K, H  
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C  
Lead Temperature (During Soldering) . . . . . +265°C  
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for  
10s Maximum

## Reliability Information

Thermal Resistance  
Ceramic DIP and FRIT Package . . . . .  $\theta_{ja}$  80°C/W  $\theta_{jc}$  20°C/W  
Flatpack Package . . . . . 70°C/W 20°C/W  
Maximum Package Power Dissipation (PD) at +125°C  
For  $T_A = -55^\circ\text{C}$  to +100°C (Package Type D, F, K) . . . . . 500mW  
For  $T_A = +100^\circ\text{C}$  to +125°C (Package Type D, F, K) . . . . . Derate  
Linearity at 12mW/°C to 200mW  
Device Dissipation per Output Transistor . . . . . 100mW  
For  $T_A = \text{Full Package Temperature Range (All Package Types)}$   
Junction Temperature . . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	μA
				2	+125°C	-	1000	μA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	μA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10μA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.  
2. Go/No Go test with limits applied to inputs.  
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

# Specifications CD40181BMS

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay A or B to F (Logic Mode), A or B to G or P	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	800	ns
			10, 11	+125°C, -55°C	-	1080	ns
Propagation Delay A or B to F, Cn+4, or A = B	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	1000	ns
			10, 11	+125°C, -55°C	-	1350	ns
Propagation Delay Cn to F	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	640	ns
			10, 11	+125°C, -55°C	-	864	ns
Propagation Delay Cn to Cn+4	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	μA
				+125°C	-	150	μA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μA
				+125°C	-	300	μA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μA
				+125°C	-	600	μA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA

# Specifications CD40181BMS

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)**

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay A or B to F (Logic Mode) A or B to G or P	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	320	ns
		VDD = 15V	1, 2, 3	+25°C	-	240	ns
Propagation Delay A or B to F, Cn+4 or A = B	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	400	ns
		VDD = 15V	1, 2, 3	+25°C	-	280	ns
Propagation Delay Cn to F	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	270	ns
		VDD = 15V	1, 2, 3	+25°C	-	200	ns
Propagation Delay Cn to Cn+4	TPHL4 TPLH4	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

**TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTND	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTPD	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

- NOTES: 1. All voltages referenced to device GND. 3. See Table 2 for +25°C limit.  
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns. 4. Read and Record

**TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C**

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

## Specifications CD40181BMS

**TABLE 6. APPLICABLE SUBGROUPS**

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

**TABLE 7. TOTAL DOSE IRRADIATION**

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

**TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS**

FUNCTION	OPEN	GROUND	VDD	9V $\pm$ -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	9-11, 13-17	1-8, 12, 18-23	24			
Static Burn-In 2 (Note 1)	9-11, 13-17	12	1-8, 18-24			
Dynamic Burn-In (Note 1)	-	4-6, 8, 12	3, 24	9-11, 13-17	1, 2, 18-23	7
Irradiation (Note 2)	9-11, 13-17	12	1-8, 18-24			

NOTES:

- Each pin except VDD and GND will have a series resistor of  $10K \pm 5\%$ , VDD =  $18V \pm 0.5V$
- Each pin except VDD and GND will have a series resistor of  $47K \pm 5\%$ ; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD =  $10V \pm 0.5V$

## Logic Diagram

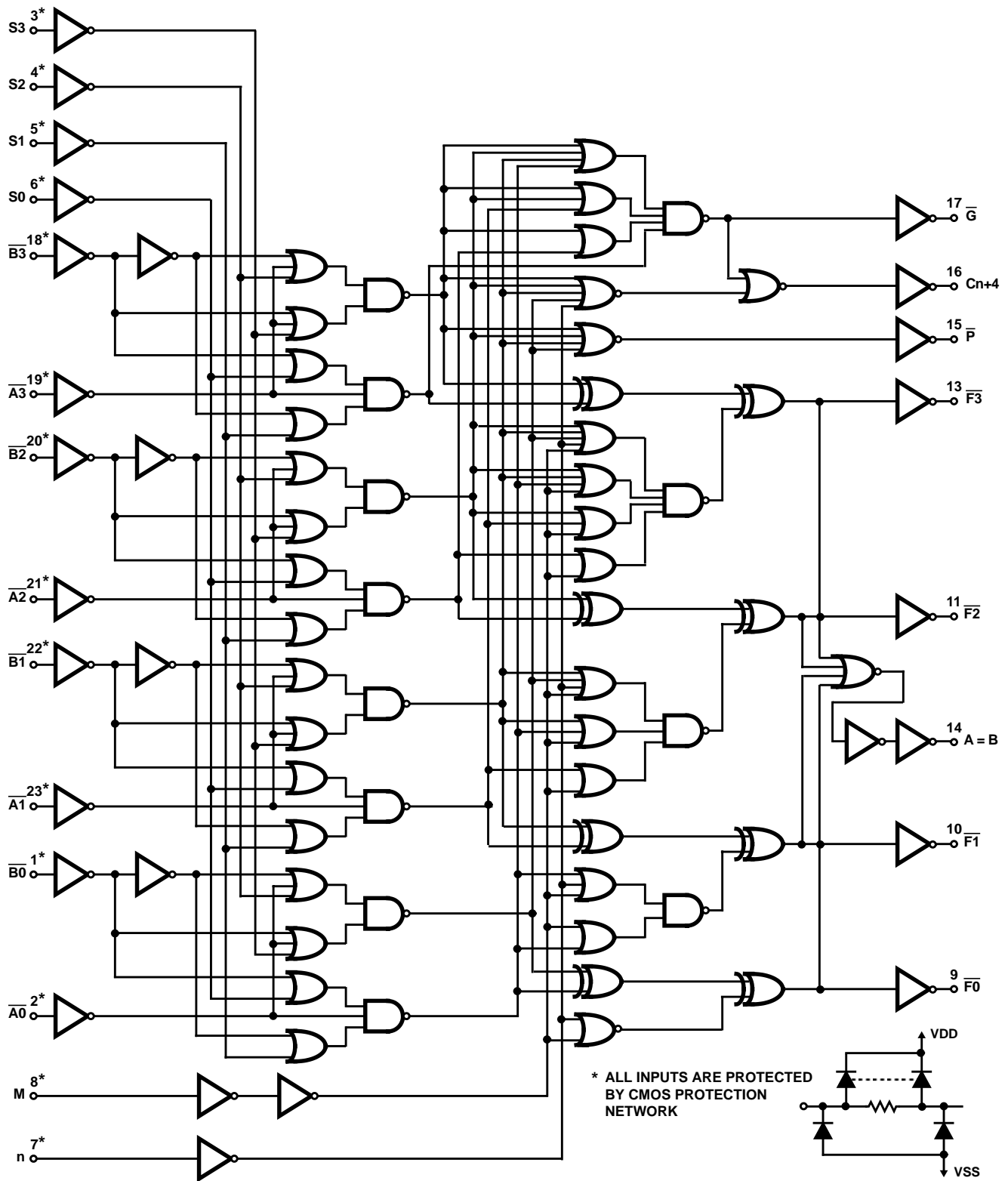


FIGURE 1. ACTIVE LOW DATA

TRUTH TABLE

FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE LOW			FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE HIGH		
				LOGIC FUNCTION M = H	ARITHMETIC* FUNCTION M = L						LOGIC FUNCTION M = H	ARITHMETIC* FUNCTION M = L	
S3	S2	S1	S0		Cn = L	Cn = H	S3	S2	S1	S0		Cn = H	Cn = L
0	0	0	0	$\overline{A}$	A minus 1	A	0	0	0	0	$\overline{A}$	A	A plus 1
0	0	0	1	$\overline{AB}$	AB minus 1	AB	0	0	0	1	$\overline{A + B}$	A + B	(A + B) plus 1
0	0	1	0	$\overline{A + B}$	$\overline{AB}$ minus 1	$\overline{AB}$	0	0	1	0	$\overline{AB}$	A + $\overline{B}$	(A + $\overline{B}$ ) plus 1
0	0	1	1	Logic 1	minus 1	Zero	0	0	1	1	Logic 0	minus 1	Zero
0	1	0	0	$\overline{A + B}$	A plus (A + $\overline{B}$ )	A plus (A + $\overline{B}$ ) plus 1	0	1	0	0	$\overline{AB}$	A plus $\overline{AB}$	A plus $\overline{AB}$ plus 1
0	1	0	1	$\overline{B}$	AB plus (A + $\overline{B}$ )	AB plus (A + $\overline{B}$ ) plus 1	0	1	0	1	$\overline{B}$	(A + B) plus $\overline{AB}$	(A + B) plus $\overline{AB}$ plus 1
0	1	1	0	$\overline{A \oplus B}$	A minus B minus 1	A minus B	0	1	1	0	$A \oplus B$	A minus B minus 1	A minus B
0	1	1	1	$\overline{A + B}$	A + $\overline{B}$	(A + $\overline{B}$ ) plus 1	0	1	1	1	$\overline{AB}$	$\overline{AB}$ minus 1	A $\overline{B}$
1	0	0	0	$\overline{AB}$	A plus (A + B)	A plus (A + B) plus 1	1	0	0	0	$\overline{A + B}$	A plus AB	A plus AB plus 1
1	0	0	1	$\overline{A \oplus B}$	A plus B	A plus B plus 1	1	0	0	1	$\overline{A \oplus B}$	A plus B	A plus B plus 1
1	0	1	0	B	$\overline{AB}$ plus (A + B)	$\overline{AB}$ plus (A + B) plus 1	1	0	1	0	B	(A + $\overline{B}$ ) plus AB	(A + $\overline{B}$ ) plus AB plus 1
1	0	1	1	A + B	A + B	A + B plus 1	1	0	1	1	AB	AB minus 1	AB
1	1	0	0	Logic 0	A plus A	A plus A plus 1	1	1	0	0	Logic 1	A plus A	A plus A plus 1
1	1	0	1	$\overline{AB}$	AB plus A	AB plus A plus 1	1	1	0	1	$\overline{A + B}$	(A + B) plus A	(A + B) plus A plus 1
1	1	1	0	AB	$\overline{AB}$ plus A	$\overline{AB}$ plus A plus 1	1	1	1	0	A + B	(A + $\overline{B}$ ) plus A	(A + $\overline{B}$ ) plus A plus 1
1	1	1	1	A	A	A plus 1	1	1	1	1	A	A minus 1	A

\* Expressed as two's complement

1 = High level

0 = Low level

## Typical Performance Characteristics

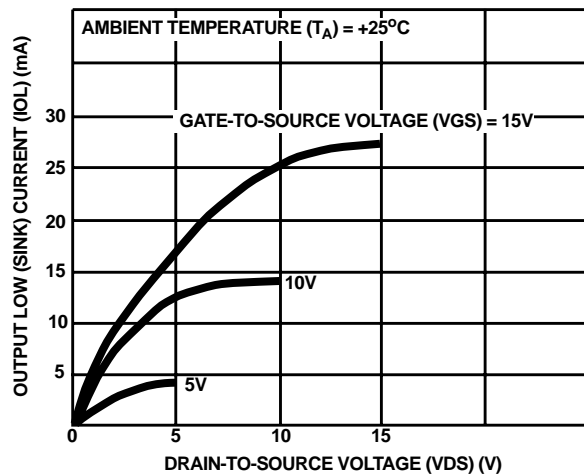


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

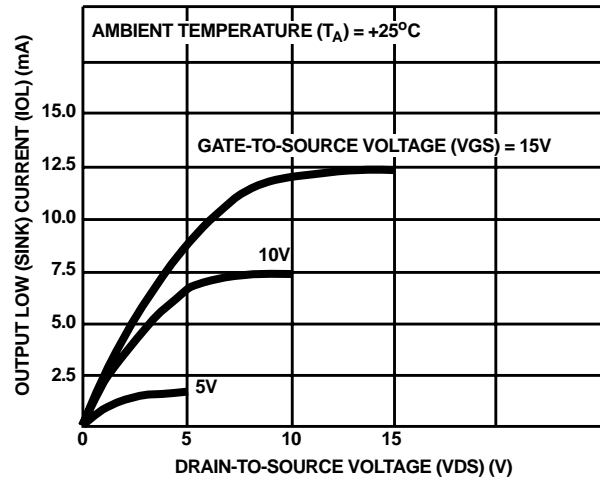


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

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# Typical Performance Characteristics (Continued)

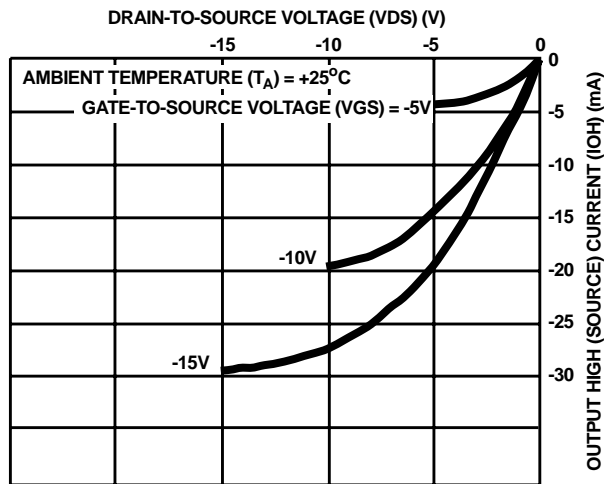


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

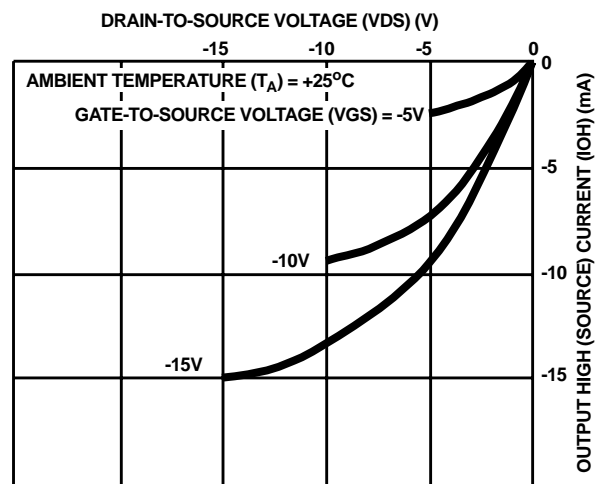


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

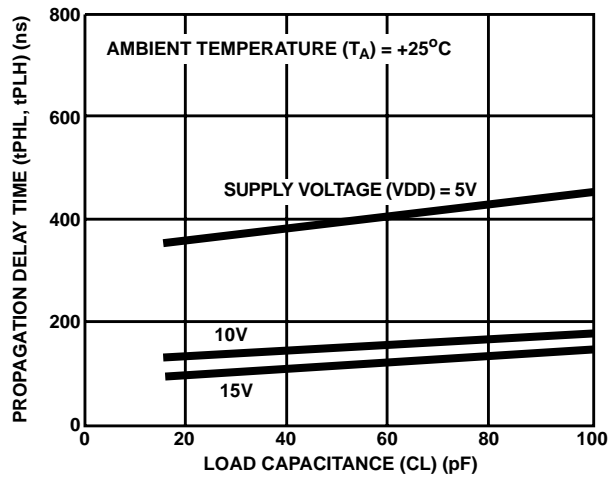


FIGURE 6. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (FOR A OR B TO F, LOGIC MODE)

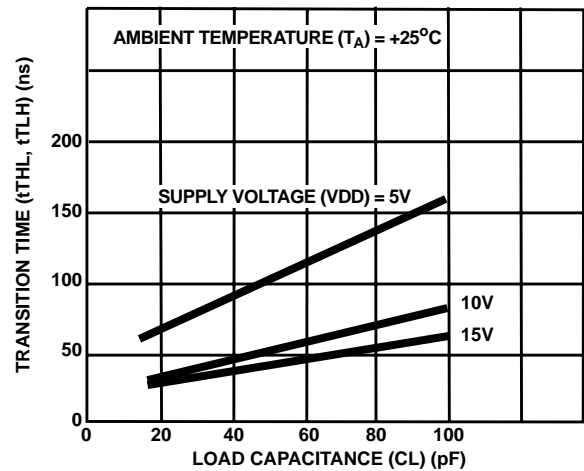


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

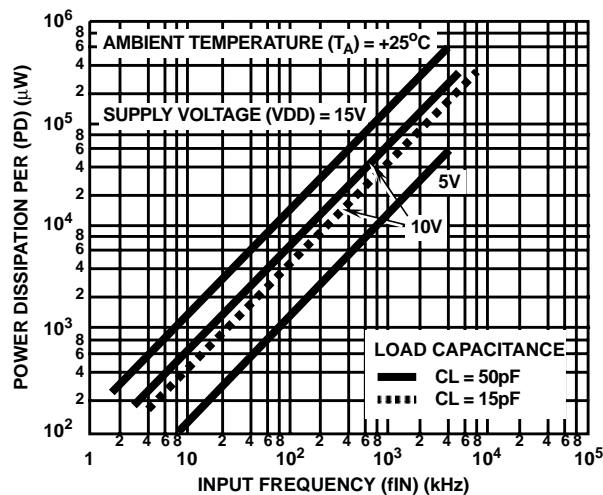


FIGURE 8. TYPICAL DYNAMIC DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

# CD40181BMS

TABLE A. AC TEST SETUP REFERENCE (ACTIVE LOW DATA)

TEST DELAY TIMES	AC PATHS		DC DATA INPUTS		MODE*
	INPUTS	OUTPUTS	TO VSS	TO VDD	
SUMIN to SUMOUT	$\overline{B0}$	Any $\overline{F}$	$\overline{B1}, \overline{B2}, \overline{B3}, M, Cn$	All $\overline{A}$ 's	Add
SUMIN to $\overline{P}$	$\overline{A0}$	$\overline{P}$	$\overline{A1}, \overline{A2}, \overline{A3}, M, Cn$	All $\overline{B}$ 's	Add
SUMIN to $\overline{G}$	$\overline{B0}$	$\overline{G}$	All $\overline{A}$ 's, M, Cn	$\overline{B1}, \overline{B2}, \overline{B3}$	Add
SUMIN to Cn+4	$\overline{B0}$	Cn+4	All $\overline{A}$ 's, M, Cn	$\overline{B1}, \overline{B2}, \overline{B3}$	Add
Cn to SUMOUT	Cn	Any $\overline{F}$	All $\overline{A}$ 's, M	All $\overline{B}$ 's	Add
Cn to Cn+4	Cn	Cn+4	All $\overline{A}$ 's, M	All $\overline{B}$ 's	Add
SUMIN to A = B	$\overline{B0}$	A = B	All $\overline{A}$ 's, B1, B2, B3, M	Cn	Subtract
SUMIN to SUMOUT (Logic Mode)	All $\overline{B}$ 's	Any $\overline{F}$	All $\overline{A}$ 's, Cn	M	Exclusive OR

\* Add Mode: S0, S3 = VDD; S1, S2 = VSS.

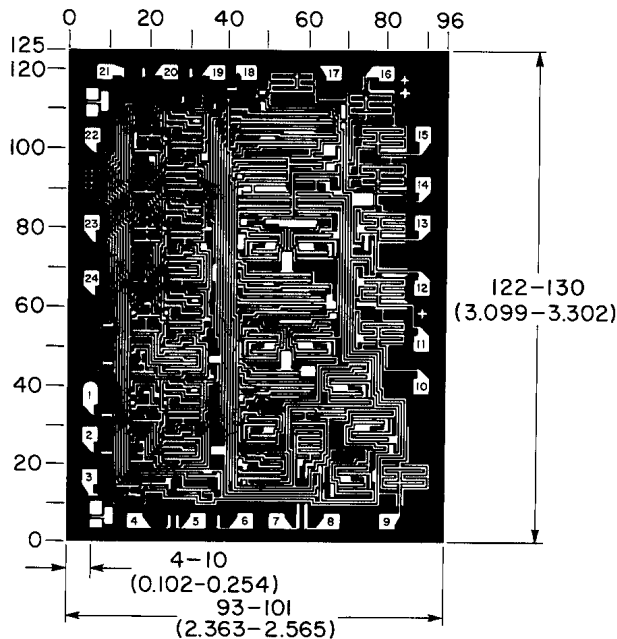
Subtract Mode: S0, S3 = VSS; S1, S2 = VDD.

TABLE B. MAGNITUDE COMPARISON

ACTIVE HIGH DATA			ACTIVE LOW DATA		
INPUT Cn	OUTPUT Cn+4	MAGNITUDE	INPUT Cn	OUTPUT Cn+4	MAGNITUDE
1	1	$A \leq B$	0	0	$A \leq B$
0	1	$A < B$	1	0	$A < B$
1	0	$A > B$	0	1	$A > B$
0	0	$A \geq B$	1	1	$A \geq B$

1 = High level 0 = Low level

## Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

**METALLIZATION:** Thickness:  $11\text{k}\text{\AA} - 14\text{k}\text{\AA}$ , AL.

**PASSIVATION:**  $10.4\text{k}\text{\AA} - 15.6\text{k}\text{\AA}$ , Silane

**BOND PADS:** 0.004 inches X 0.004 inches MIN

**DIE THICKNESS:** 0.0198 inches - 0.0218 inches