

FSDL0165RN

Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged Sense FET
- Consumes only 0.65W at 240VAC & 0.3W load with Advanced Burst-Mode Operation
- Frequency Modulation for low EMI
- Precision Fixed Operating Frequency
- Internal Start-up Circuit
- Pulse by Pulse Current Limiting
- Abnormal Over Current Protection
- Over Voltage Protection
- Over Load Protection
- Internal Thermal Shutdown Function
- Auto-Restart Mode
- Under Voltage Lockout
- Low Operating Current (3mA)
- Adjustable Peak Current Limit
- Built-in Soft Start

Applications

- SMPS for VCR, SVR, STB, DVD & DVCD
- SMPS for Printer, Facsimile & Scanner
- Adaptor for Camcorder

Description

The FSDL0165RN is an integrated Pulse Width Modulator (PWM) and Sense FET specifically designed for high performance offline Switch Mode Power Supplies (SMPS) with minimal external components. This device is an integrated high voltage power switching regulator which combine an avalanche rugged Sense FET with a current mode PWM control block. The integrated PWM controller features include: a fixed oscillator with frequency modulation for reduced EMI, Under Voltage Lock Out (UVLO) protection, Leading Edge Blanking (LEB), optimized gate turn-on/turn-off driver, Thermal Shut Down (TSD) protection, Abnormal Over Current Protection (AOCP) and temperature compensated precision current sources for loop compensation and fault protection circuitry. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSDL0165RN reduce total component count, design size, weight and at the same time increases efficiency, productivity, and system reliability. This device is a basic platform well suited for cost effective designs of flyback converters.

| OUTPUT POWER TABLE | | | | |
|--------------------|----------------------------------|---------------------------|-------------------------|---------------------------|
| PRODUCT | 230VAC $\pm 15\%$ ⁽³⁾ | | 85-265VAC | |
| | Adapt-er ⁽¹⁾ | Open Frame ⁽²⁾ | Adapt-er ⁽¹⁾ | Open Frame ⁽²⁾ |
| FSDL321 | 11W | 17W | 8W | 12W |
| FSDH321 | 11W | 17W | 8W | 12W |
| FSDL0165RN | 13W | 23W | 11W | 17W |
| FSDM0265RN | 16W | 27W | 13W | 20W |
| FSDH0265RN | 16W | 27W | 13W | 20W |
| FSDL0365RN | 19W | 30W | 16W | 24W |
| FSDM0365RN | 19W | 30W | 16W | 24W |
| FSDL0165RL | 13W | 23W | 11W | 17W |
| FSDM0265RL | 16W | 27W | 13W | 20W |
| FSDH0265RL | 16W | 27W | 13W | 20W |
| FSDL0365RL | 19W | 30W | 16W | 24W |
| FSDM0365RL | 19W | 30W | 16W | 24W |

Table 1. Notes: 1. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient. 2. Maximum practical continuous power in an open frame design at 50°C ambient. 3. 230 VAC or 100/115 VAC with doubler.

Typical Circuit

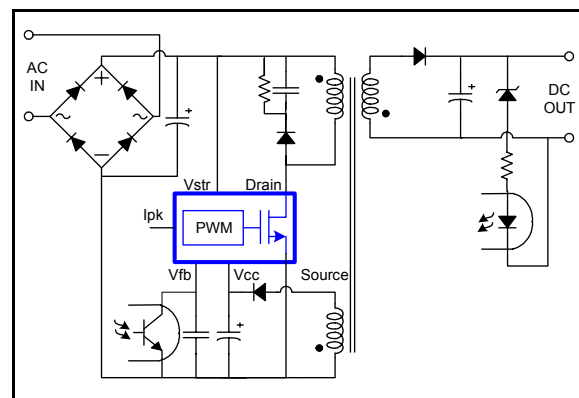


Figure 1. Typical Flyback Application

Internal Block Diagram

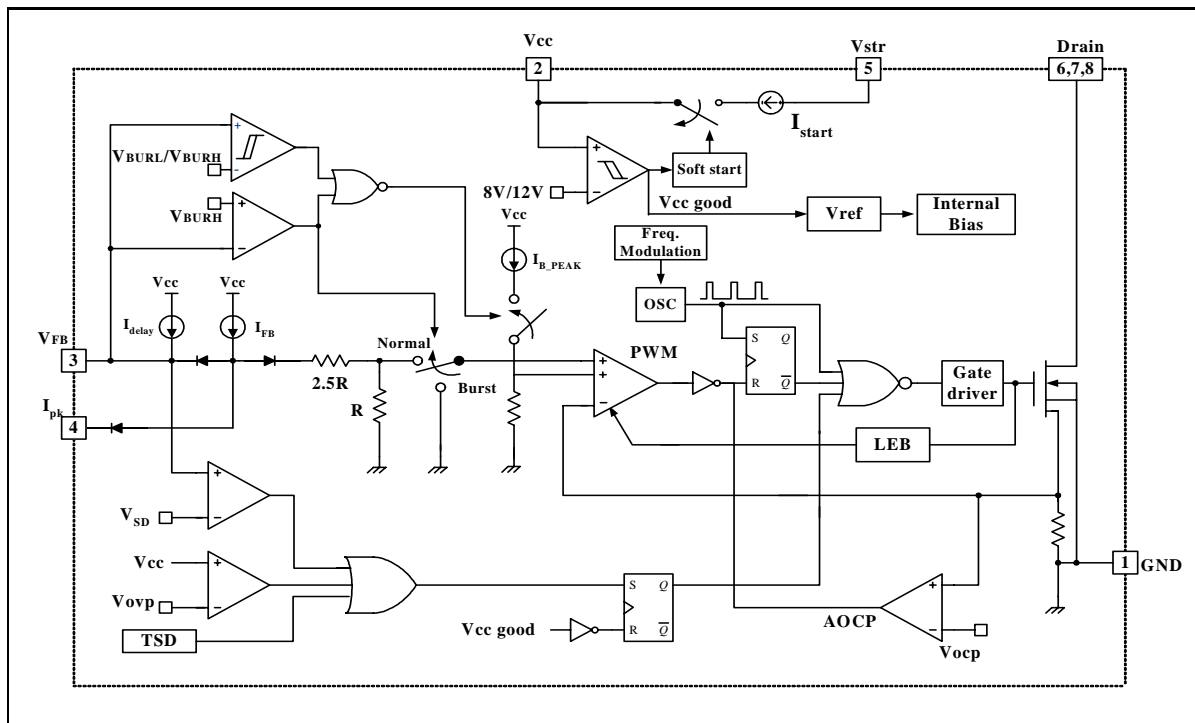


Figure 2. Functional Block Diagram of FSDL0165RN

Pin Definitions

| Pin Number | Pin Name | Pin Function Description |
|------------|----------|--|
| 1 | GND | Sense FET source terminal on primary side and internal control ground. |
| 2 | Vcc | Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during startup (see Internal Block Diagram section). It is not until Vcc reaches the UVLO upper threshold (12V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding. |
| 3 | Vfb | The feedback voltage pin is the non-inverting input to the PWM comparator. It has a 0.9mA current source connected internally while a capacitor and optocoupler are typically connected externally. A feedback voltage of 6V triggers over load protection (OLP). There is a time delay while charging between 3V and 6V using an internal 5uA current source, which prevents false triggering under transient conditions but still allows the protection mechanism to operate under true overload conditions. |
| 4 | Ipk | Pin to adjust the current limit of the Sense FET. The feedback 0.9mA current source is diverted to the parallel combination of an internal 2.8kΩ resistor and any external resistor to GND on this pin to determine the current limit. If this pin is tied to Vcc or left floating, the typical current limit will be 1.2A. |
| 5 | Vstr | This pin connects directly to the rectified AC line voltage source. At start up the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the Vcc reaches 12V, the internal switch is disabled. |
| 6, 7, 8 | Drain | The Drain pin is designed to connect directly to the primary lead of the transformer and is capable of switching a maximum of 650V. Minimizing the length of the trace connecting this pin to the transformer will decrease leakage inductance. |

Pin Configuration

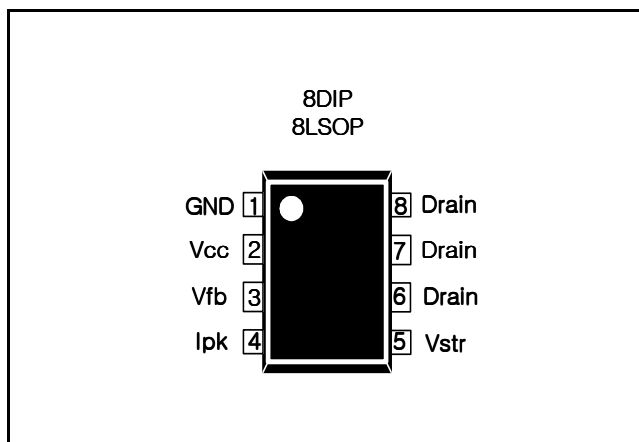


Figure 3. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

| Characteristic | Symbol | Value | Unit |
|---|---------------------|-------------------------|------|
| Drain Current Pulsed ⁽¹⁾ | I _{DM} | 4.0 | ADC |
| Single Pulsed Avalanche Energy ⁽²⁾ | EAS | 95 | mJ |
| Maximum Supply Voltage | V _{CC,MAX} | 20 | V |
| Analog Input Voltage Range | V _{FB} | -0.3 to V _{SD} | V |
| Total Power Dissipation | P _D | 1.25 | W |
| Operating Junction Temperature. | T _J | +150 | °C |
| Operating Ambient Temperature. | T _A | -25 to +85 | °C |
| Storage Temperature Range. | T _{STG} | -55 to +150 | °C |

Note:

1. Repetitive rating: Pulse width limited by maximum junction temperature
2. L = 51mH, starting T_j = 25°C
3. L = 13μH, starting T_j = 25°C
4. V_{sd} is shutdown feedback voltage (see Protection Section in Electrical Characteristics)

Thermal Impedance

| Parameter | Symbol | Value | Unit |
|-----------------------------|--------------------------------|-------|---------------------|
| 8DIP | | | |
| Junction-to-Ambient Thermal | θ _{JA} ⁽¹⁾ | 81.50 | °C/W ⁽³⁾ |
| Junction-to-Case Thermal | θ _{JC} ⁽²⁾ | 21.90 | °C/W |

Note:

1. Free standing with no heatsink.
2. Measured on the GND pin close to plastic interface.
3. Soldered to 0.36 sq. inch(232mm²), 2 oz.(610g/m²) copper clad.

Electrical Characteristics

(Ta = 25°C unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---------|--|------|------|------|------|
| Sense FET SECTION | | | | | | |
| Startup Voltage (Vstr) Breakdown | BVSTR | VCC=0V, ID=1mA | 650 | - | - | V |
| Drain-Source Breakdown Voltage | BVDSS | VGS=0V, ID=50μA | 650 | - | - | V |
| Off-State Current (Max.Rating =660V) | IDSS | VDS=660V, VGS=0V | - | - | 50 | μA |
| | | VDS=0.8Max.Rating VGS=0V, TC=125°C | - | - | 200 | μA |
| On-State Resistance(1) | RDS(ON) | VGS=10V, ID=0.5A | - | 8.0 | 10.0 | Ω |
| Input Capacitance | CISS | VGS=0V, VDS=25V, F=1MHz | - | 250 | - | pF |
| Output Capacitance | COSS | | - | 25 | - | pF |
| Reverse Transfer Capacitance | CRSS | | - | 10 | - | pF |
| Turn On Delay Time | TD(ON) | VDS=325V, ID=1.0A (Sense FET switching time is essentially independent of operating temperature) | - | 12 | - | ns |
| Rise Time | TR | | - | 4 | - | ns |
| Turn Off Delay Time | TD(OFF) | | - | 30 | - | ns |
| Fall Time | TF | | - | 10 | - | ns |
| CONTROL SECTION | | | | | | |
| Output Frequency | FOSC | FSDL0165R | 45 | 50 | 55 | KHz |
| Output Frequency Modulation | FMOD | | ±1.0 | ±1.5 | ±2.0 | KHz |
| Frequency Change With Temperature(2) | - | -25°C ≤ Ta ≤ 85°C | - | ±5 | ±10 | % |
| Maximum Duty Cycle | DMAX | FSDL0165R | 71 | 77 | 83 | % |
| Minimum Duty Cycle | DMIN | | 0 | 0 | 0 | % |
| Start threshold voltage | VSTART | VFB=GND | 11 | 12 | 13 | V |
| Stop threshold voltage | VSTOP | VFB=GND | 7 | 8 | 9 | V |
| Feedback Source Current | IFB | VFB=GND | 0.7 | 0.9 | 1.1 | mA |
| Internal Soft Start Time | TS/S | VFB=4V | 10 | 15 | 20 | ms |
| BURST MODE SECTION | | | | | | |
| Burst Mode Voltages | VBURH | - | 0.5 | 0.6 | 0.7 | V |
| | VBURL | - | 0.25 | 0.35 | 0.45 | V |
| PROTECTION SECTION | | | | | | |
| Drain to Source Peak Current Limit | IOVER | Max. inductor current | 1.06 | 1.20 | 1.35 | A |
| Current Limit Delay(3) | TCLD | | - | 500 | - | ns |
| Thermal Shutdown | TSD | - | 125 | 140 | - | °C |

| | | | | | | |
|---------------------------------|--------|---------|-----|------|-----|----|
| Shutdown Feedback Voltage | VSD | | 5.5 | 6.0 | 6.5 | V |
| Over Voltage Protection | VOVP | | 18 | 19 | - | V |
| Shutdown Feedback Delay Current | IDELAY | VFB=4V | 3.5 | 5.0 | 6.5 | μA |
| Leading Edge Blanking Time | TLEB | | 200 | - | - | ns |
| TOTAL DEVICE SECTION | | | | | | |
| Operating Current | IOP | VCC=14V | 1 | 3 | 5 | mA |
| Start Up Current | ISTART | VCC=0V | 0.7 | 0.85 | 1.0 | mA |
| Vstr Supply Voltage | VSTR | VCC=0V | 35 | - | - | V |

Note:

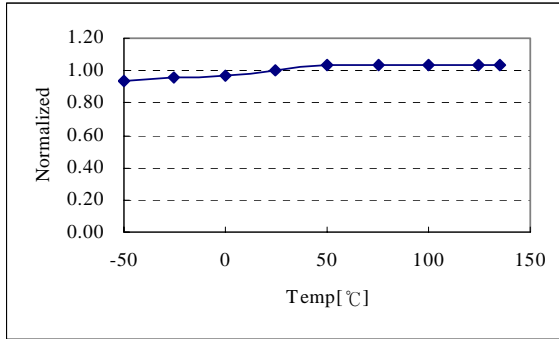
1. Pulse test: Pulse width $\leq 300\mu\text{s}$, duty $\leq 2\%$
2. These parameters, although guaranteed, are tested in EDS (wafer test) process
3. These parameters, although guaranteed, are not 100% tested in production

Comparison Between KA5x0165RN and FSDL0165RN

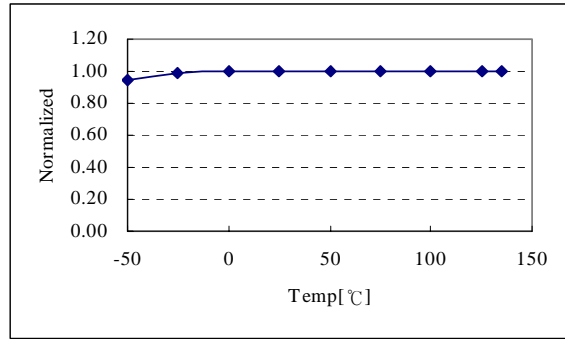
| Function | KA5x0265RN | FSDL0165RN | FSDL0165RN Advantages |
|---------------------------|----------------|---------------------------------------|---|
| Soft-Start | not applicable | 15mS | <ul style="list-style-type: none"> • Gradually increasing current limit during soft-start further reduces peak current and voltage component stresses • Eliminates external components used for soft-start in most applications • Reduces or eliminates output overshoot |
| External Current Limit | not applicable | Programmable of default current limit | <ul style="list-style-type: none"> • Smaller transformer • Allows power limiting (constant over-load power) • Allows use of larger device for lower losses and higher efficiency. |
| Frequency Modulation | not applicable | $\pm 1.5\text{KHz @}50\text{KHz}$ | <ul style="list-style-type: none"> • Reduced conducted EMI |
| Burst Mode Operation | not applicable | Yes-built into controller | <ul style="list-style-type: none"> • Improve light load efficiency • Reduces no-load consumption • Transformer audible noise reduction |
| Drain Creepage at Package | 1,02mm | 7.62mm | <ul style="list-style-type: none"> • Greater immunity to arcing as a result of build-up of dust, debris and other contaminants |

Typical Performance Characteristics (Control Part)

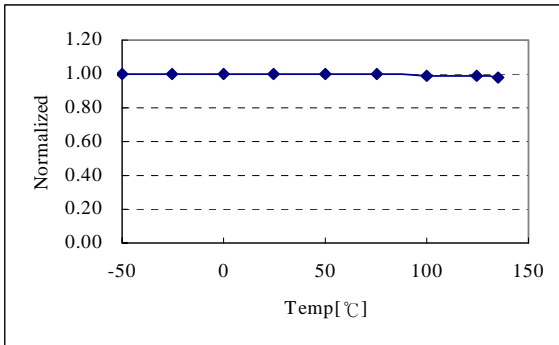
(These characteristic graphs are normalized at $T_a = 25^{\circ}\text{C}$)



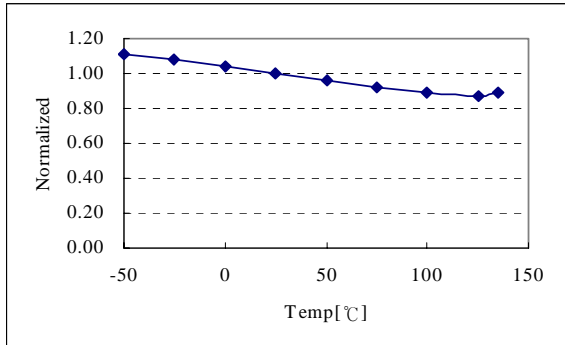
Operating Frequency (Fosc)



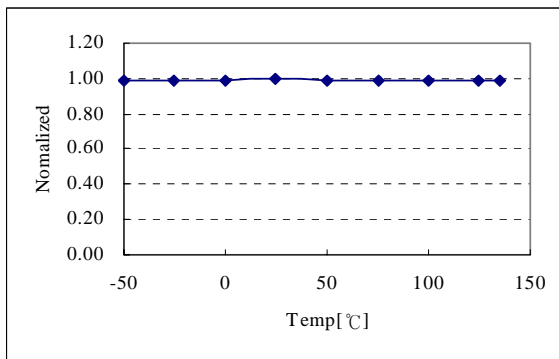
Frequency Modulation (Fmod)



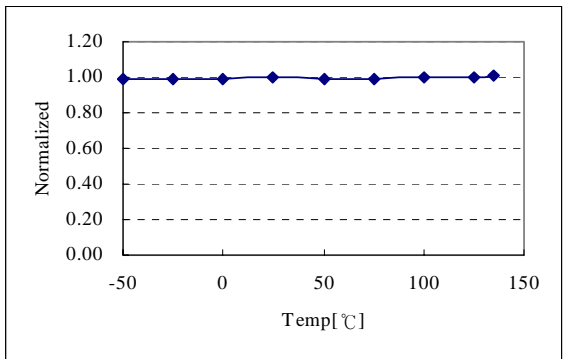
Maximum duty cycle (Dmax)



Operating supply current (Iop)

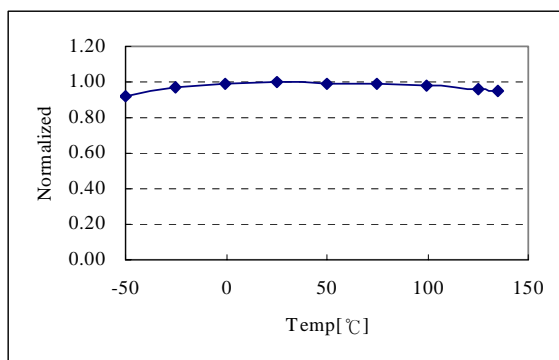
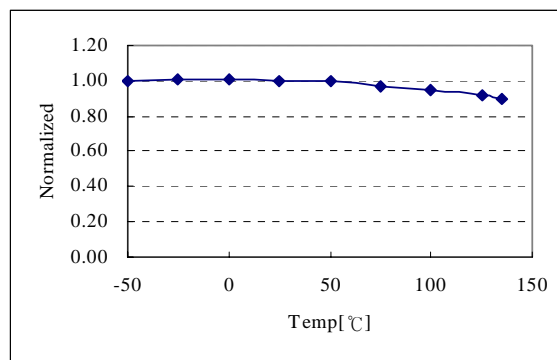
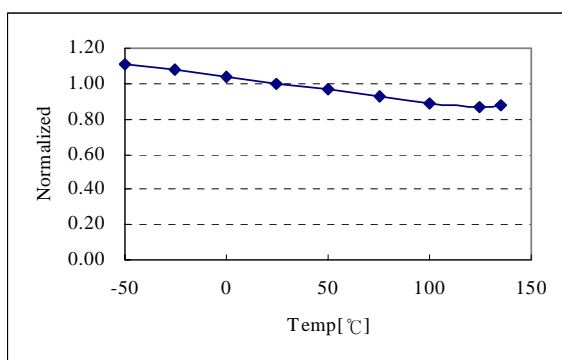
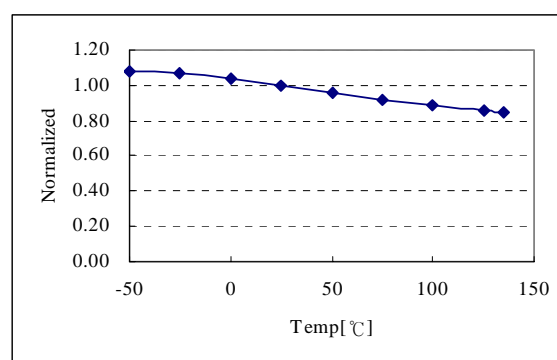
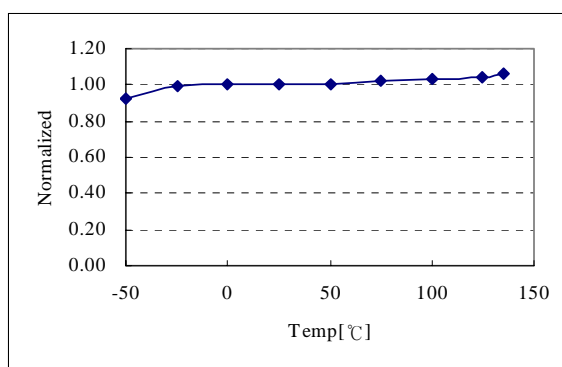
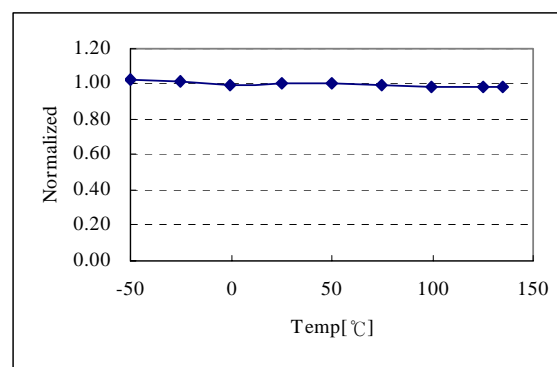


Start Threshold Voltage (Vstart)



Stop Threshold Voltage (Vstop)

Typical Performance Characteristics (Continued)

**Feedback Source Current (Ifb)****Peak current limit (Iover)****Start up Current (Istart)****J-FET Start up current (Istr)****Burst peak current (Iburst)****Over Voltage Protection (Vovp)**

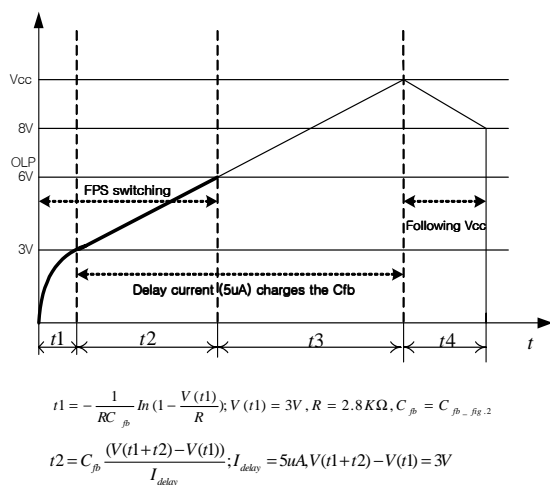


Figure 6. Over load protection

4.2 Thermal Shutdown (TSD) : The Sense FET and the control IC are integrated, making it easier for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 140°C, thermal shutdown is activated.

4.3 Abnormal Over Current Protection (AOCP) :

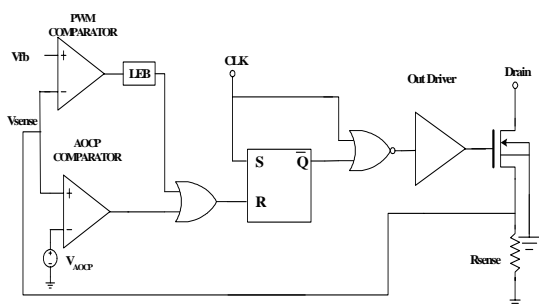


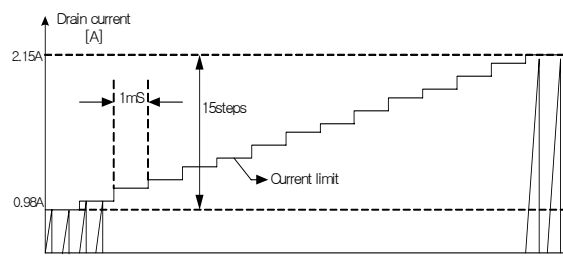
Figure 7. AOCP Function & Block

Even though the FPSTM has OLP (Over Load Protection) and current mode PWM feedback, these are not enough to protect the FPSTM when a secondary side diode short or a transformer pin short occurs. In addition to start-up, soft-start is also activated at each restart attempt during auto-restart and when restarting after latch mode is activated. The FPSTM has an internal AOCP (Abnormal Over Current Protection) circuit as shown in figure 7. When the gate turn-on signal is applied to the power Sense FET, the AOCP block is

enabled and monitors the current through the sensing resistor. The voltage across the resistor is then compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, pulse by pulse AOCP is triggered regardless of uncontrollable LEB time. Here, pulse by pulse AOCP stops Sense FET within 350nS after it is activated.

4.4 Over Voltage Protection (OVP) : In case of malfunction in the secondary side feedback circuit, or feedback loop open caused by a defect of solder, the current through the opto-coupler transistor becomes almost zero. Then, Vfb climbs up in a similar manner to the over load situation, forcing the preset maximum current to be supplied to the SMPS until the over load protection is activated. Because excess energy is provided to the output, the output voltage may exceed the rated voltage before the over load protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. In general, Vcc is proportional to the output voltage and the FPSTM uses Vcc instead of directly monitoring the output voltage. If Vcc exceeds 19V, OVP circuit is activated resulting in termination of the switching operation. In order to avoid undesired activation of OVP during normal operation, Vcc should be properly designed to be below 19V.

5. Soft Start : The FPSTM has an internal soft start circuit that increases the feedback voltage together with the Sense FET current slowly after it starts up. The typical soft start time is 15msec, as shown in figure 8, where progressive increments of Sense FET current are allowed during the start-up phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode.



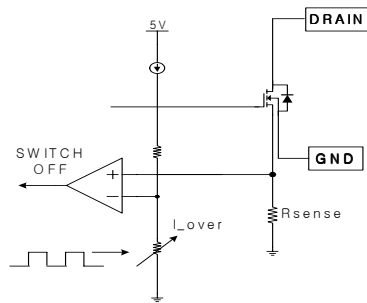


Figure 8. Soft Start Function

6. Burst operation : In order to minimize power dissipation in standby mode, the FPSTM enters burst mode operation.

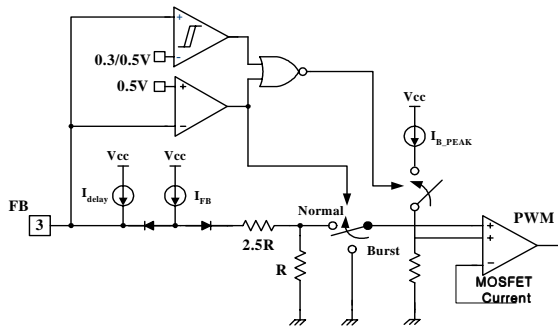


Figure 9. Circuit for Burst operation

As the load decreases, the feedback voltage decreases. As shown in figure 10, the device automatically enters burst mode when the feedback voltage drops below V_{BURH} (500mV). Switching still continues but the current limit is set to a fixed limit internally to minimize flux density in the transformer. The fixed current limit is larger than that defined by $V_{fb} = V_{BURH}$ and therefore, V_{fb} is driven down further. Switching continues until the feedback voltage drops below V_{BURL} (300mV). At this point switching stops and the output voltages start to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (500mV) switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the power Sense FET thereby reducing switching loss in Standby mode.

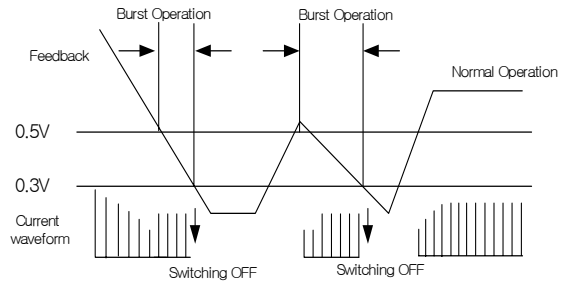


Figure 10. Circuit for Burst Operation

7. Frequency Modulation : EMI reduction can be accomplished by modulating the switching frequency of a switched power supply. Frequency modulation can reduce EMI by spreading the energy over a wider frequency range than the band width measured by the EMI test equipment. The amount of EMI reduction is directly related to the depth of the reference frequency. As can be seen in Figure 11, the frequency changes from 65KHz to 69KHz in 4mS for the FSDM0265RN. Frequency modulation allows the use of a cost effective inductor instead of an AC input mode choke to satisfy the requirements of world wide EMI limits.

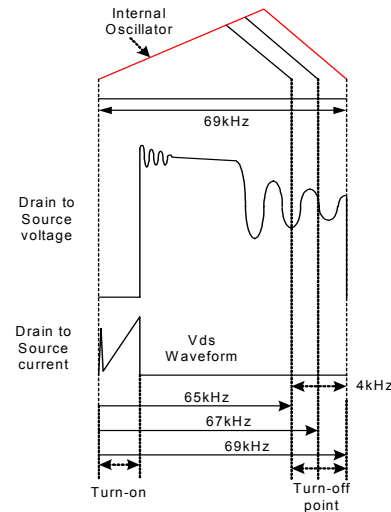


Figure 11. Frequency Modulation Waveform

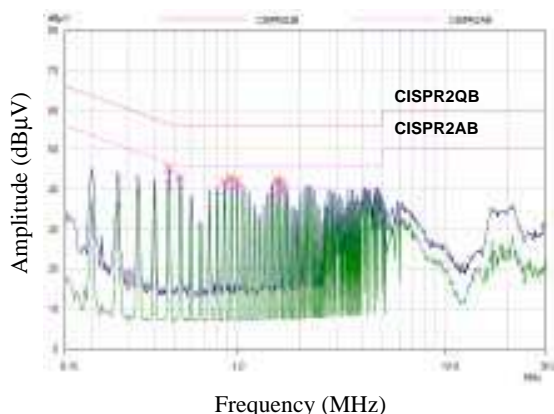


Figure 12. KA5-series FPS™ Full Range EMI scan(67KHz, no Frequency Modulation) with DVD Player SET

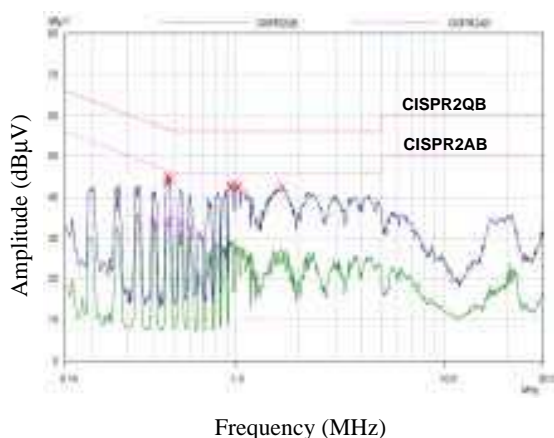


Figure 13. FSDX-series FPS™ Full Range EMI Scan (67KHz, with Frequency Modulation) with DVD Player SET

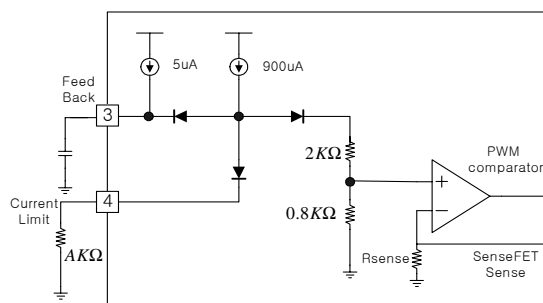


Figure 14. Peak current adjustment

For example, FSDx0265RN has a typical Sense FET current limit (IOVER) of 2.15A. The Sense FET current can be limited to 1A by inserting a 2.8kΩ between the current limit pin and ground which is derived from the following equations:

$$2.15: 1 = 2.8K\Omega : XK\Omega,$$

$$X = 1.3K\Omega,$$

Since X represents the resistance of the parallel network, Y can be calculated using the following equation:

$$Y = X / (1 - (X/2.8K\Omega))$$

8. Adjusting Current limit function: As shown in fig 14, a combined 2.8KΩ internal resistance is connected into the non-inverting lead on the PWM comparator. A external resistance of Y on the current limit pin forms a parallel resistance with the 2.8KΩ when the internal diodes are biased by the main current source of 900uA.

Typical application circuit

1. Set Top Box Example Circuit (13W Output Power)

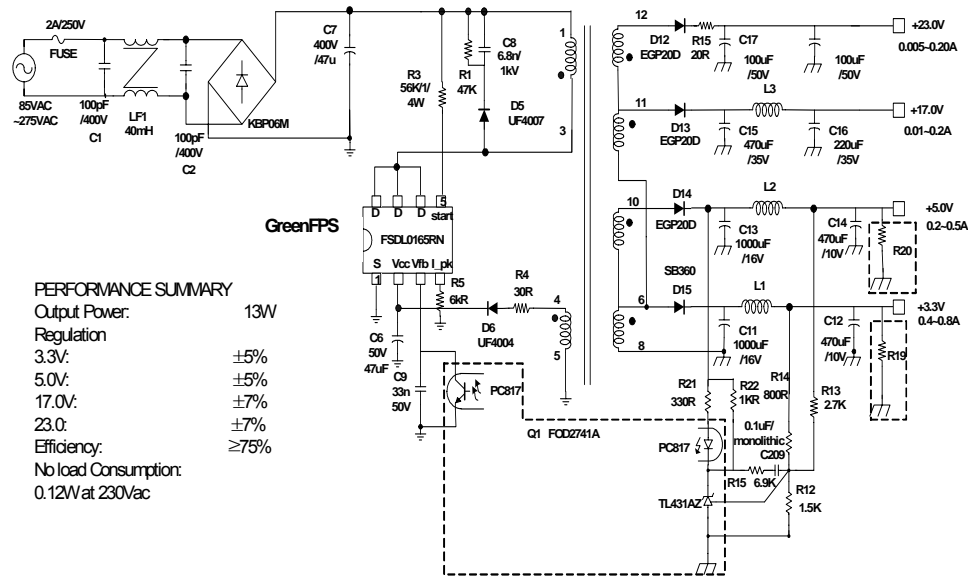


Figure15. 13W multiple power supply using FSDL0165RN

Multiple Output, 13W, 85-265VAC Input Power supply:

Figure 15 shows a multiple output supply typical for high end set-top boxes containing high capacity hard disks for recording. The supply delivers an output power of 13W cont./15W peak (thermally limited) from an input voltage of 85 to 265 VAC. Efficiency at 9W, 85VAC is ≥75%.

The 3.3 V and 5 V outputs are regulated to ±5% without the need for secondary linear regulators. DC stacking (the secondary winding reference for the other output voltages is connected to the anode of D15. For more accuracy, connection to the cathode of D15 will be better.) is used to minimize the voltage error for the higher voltage outputs. Due to the high ambient operating temperature requirement typical of a set-top box (60 °C) the FSDL0165RN is used to reduce conduction losses without a heatsink. Resistor R5 sets the device current limit to limit overload power.

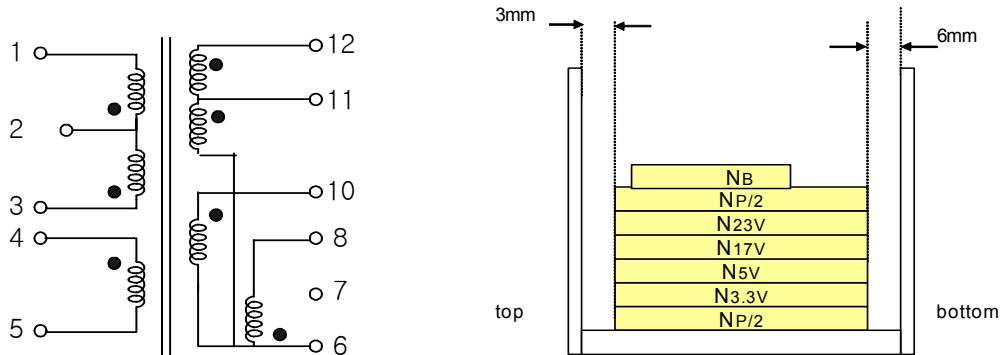
Leakage inductance clamping is provided by R1 and C8, keeping the DRAIN voltage below 650 V under all conditions. Resistor R1 and capacitor C8 are selected such that R1 dissipates power to prevent rising of DRAIN Voltage caused by leakage inductance. The frequency modulation feature of FSDL0165RN allows the circuit shown to meet CISPR2AB with simple EMI filtering (C1, LF1 and C2) and the output grounded. The secondaries are rectified and smoothed by D12, D13, D14, and D15. Diode D15 for the 3.4V output is a Schottky diode to maximize efficiency. Diode D14 for the 5 V output is a PN type to center the 5 V output at 5 V. The 3.3 V and 5 V output voltage require two capacitors in parallel to meet the ripple current requirement. Switching noise filtering is provided by L3, L2 and L1. Resistor R15 prevents

peak charging of the lightly loaded 23V output. The outputs are regulated by the reference (TL431) voltage in secondary. Both the 3.3 V and 5 V outputs are sensed via R13 and R14. Resistor R22 provides bias for TL431 and R21 sets the overall DC gain. Resistor R21, C209, R14 and R13 provide loop compensation.

2. Transformer Specification

1. TRANSFORMER SPECIFICATION

- SCHEMATIC DIAGRAM (TRANSFORMER)



2. WINDING SPECIFICATION

| NO. | PIN(S → F) | WIRE | TURNS | WINDING METHOD |
|-------|------------|----------------------|-------|------------------|
| NP/2 | 3 → 2 | 0.25 $\Phi \times 1$ | 22 | SOLENOID WINDING |
| N3.3V | 6 → 8 | 0.3 $\Phi \times 8$ | 2 | STACK WINDING |
| N5V | 10 → 6 | 0.3 $\Phi \times 2$ | 1 | STACK WINDING |
| N16V | 11 → 6 | 0.3 $\Phi \times 4$ | 7 | SOLENOID WINDING |
| N23V | 12 → 11 | 0.3 $\Phi \times 2$ | 3 | SOLENOID WINDING |
| NP/2 | 2 → 1 | 0.25 $\Phi \times 1$ | 22 | SOLENOID WINDING |
| NB | 4 → 5 | 0.25 $\Phi \times 1$ | 10 | CENTER WINDING |

3. ELECTRIC CHARACTERISTIC

| CLOSURE | PIN | SPEC. | REMARKS |
|------------|-------|-----------------|---------------|
| INDUCTANCE | 1 - 3 | 800uH \pm 10% | 1KHz, 1V |
| LEAKAGE L | 1 - 3 | 15uH MAX. | 2nd ALL SHORT |

4. BOBBIN & CORE.

CORE: EER2828
BOBBIN: EER2828

Layout Considerations

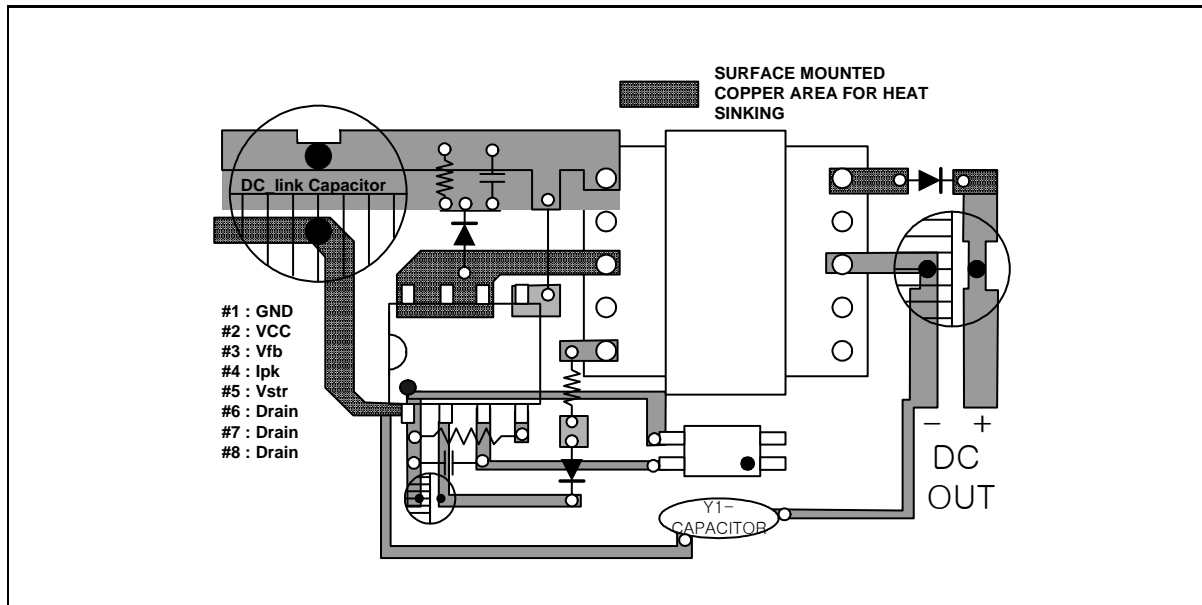
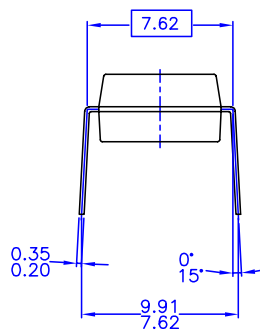
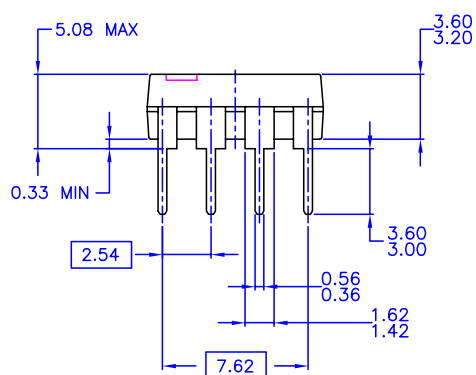
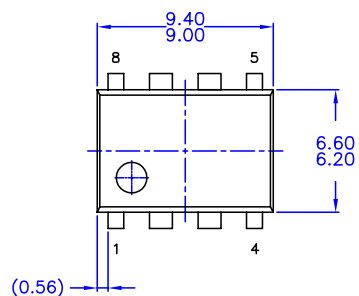


Figure 15. Layout Considerations for FSDL0165RN using 8DIP

Package Dimensions

8DIP

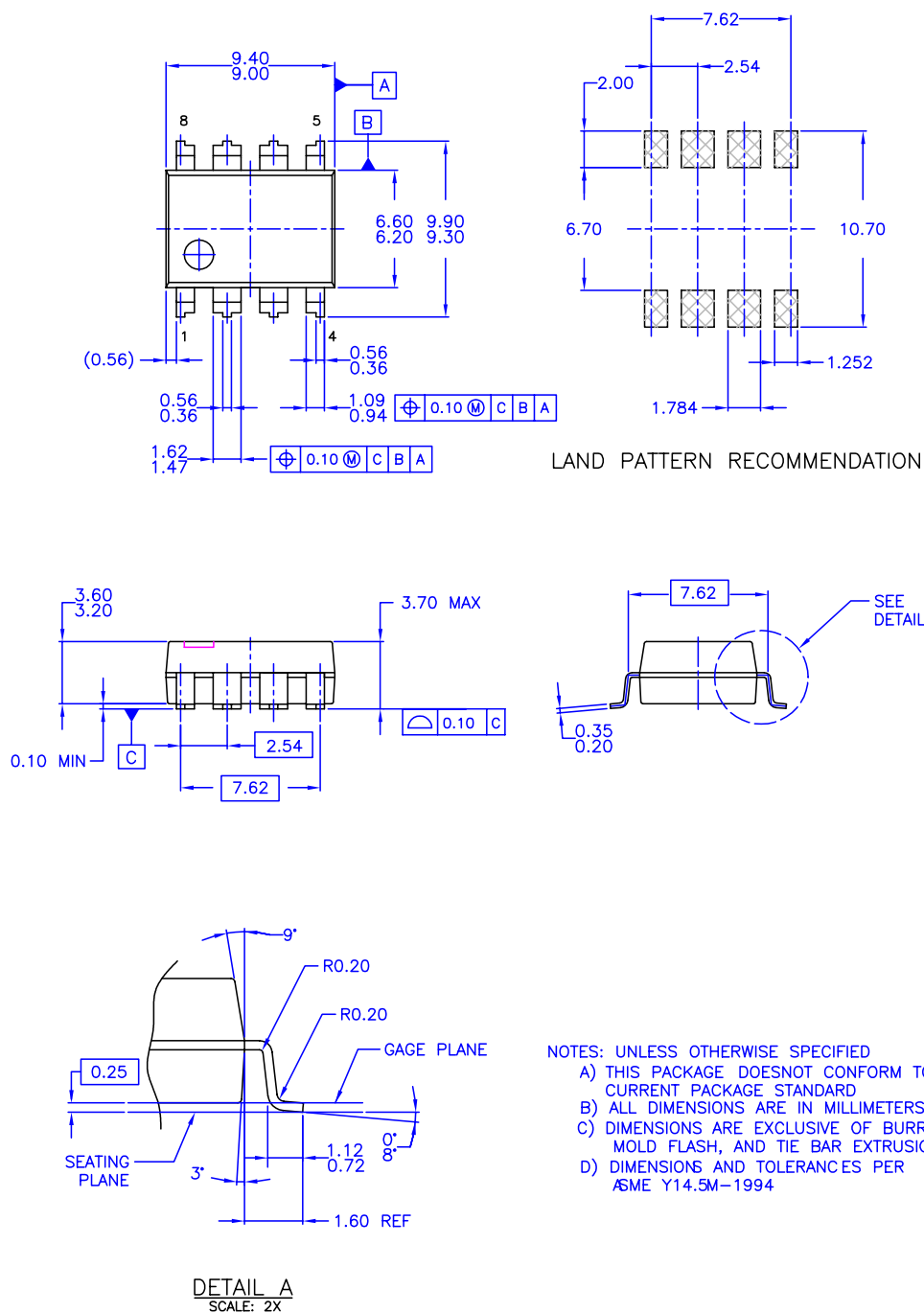


NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

Package Dimensions (Continued)

8LSOP



Ordering Information

| Product Number | Package | Marking Code | BV _{DSS} | F _{OSC} | R _{DS(on)} |
|----------------|---------|--------------|-------------------|------------------|---------------------|
| FSDL0165RN | 8DIP | DL0165R | 650V | 50KHz | 8.0Ω |
| FSDL0165RL | 8LSOP | DL0165R | 650V | 50KHz | 8.0Ω |

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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