TOSHIBA TRANSISTOR SILICON NPN TRIPLE DIFFUSED MESA TYPE

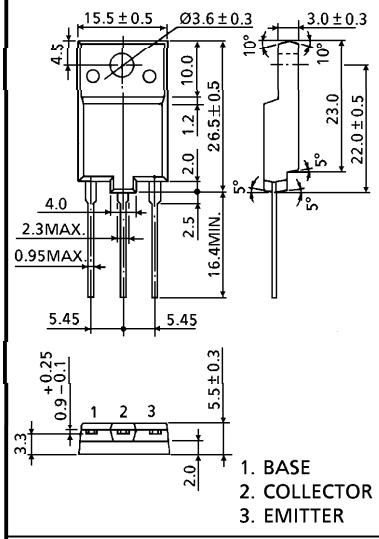
2SD2553

HORIZONTAL DEFLECTION OUTPUT FOR HIGH RESOLUTION DISPLAY, COLOR TV

HIGH SPEED SWITCHING APPLICATIONS

- High Voltage : V_{CBO} = 1700 V
- Low Saturation Voltage : $V_{CE\ (sat)}$ = 5 V (Max.)
- High Speed : t_f = 0.3 μs (Typ.)
- Bult-in Damper Type
- Collector Metal (Fin) is Fully Covered with Mold Resin.

Unit in mm



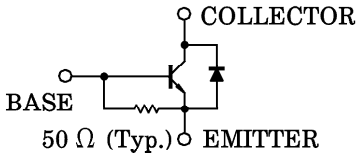
JEDEC	—
EIAJ	—
TOSHIBA	2-16E3A

Weight : 5.5 g (Typ.)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Collector-Base Voltage		V_{CBO}	1700	V
Collector-Emitter Voltage		V_{CEO}	600	V
Emitter-Base Voltage		V_{EBO}	5	V
Collector Current	DC	I_C	8	A
	Pulse	I_{CP}	16	
Base Current		I_B	4	A
Collector Power Dissipation (Tc = 25°C)		P_C	50	W
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_{stg}	−55~150	°C

EQUIVALENT CIRCUIT



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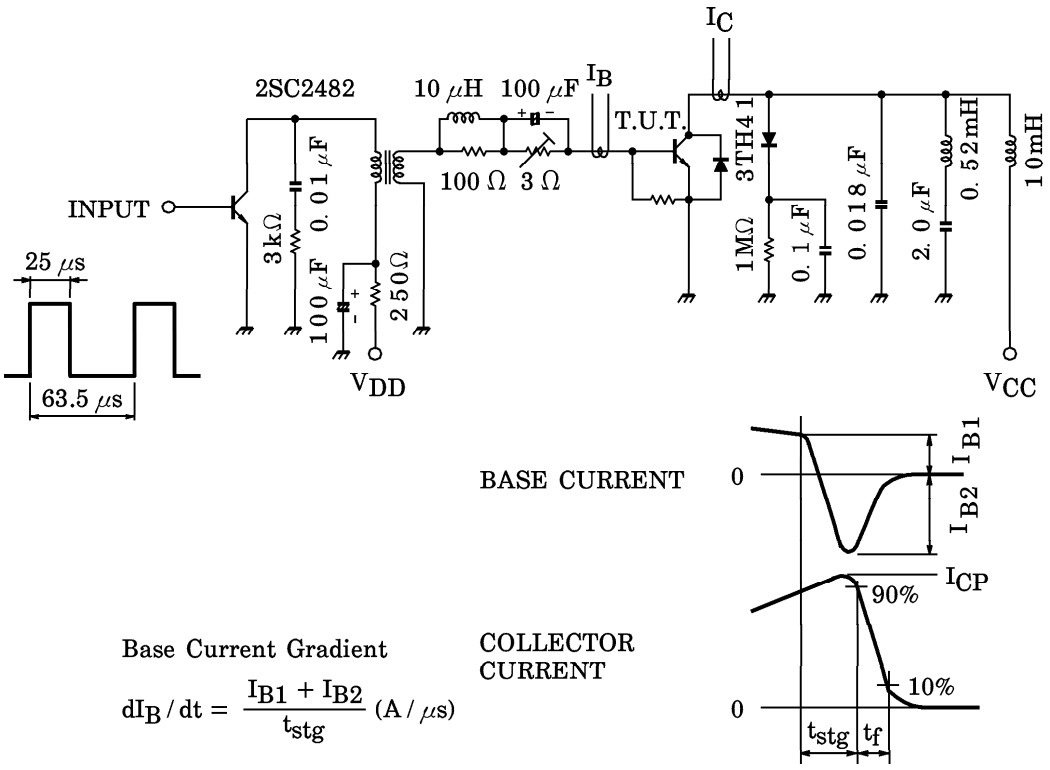
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut-off Current		I_{CBO}	V_{CB} = 1700 V, I_E = 0	—	—	1	mA
Emitter Cut-off Current		I_{EBO}	V_{EB} = 5 V, I_C = 0	66	—	200	mA
Emitter-Base Breakdown Voltage		V_{EBO}	I_E = 400 mA, I_C = 0	5	—	—	V
DC Current Gain		$h_{FE\,(1)}$	V_{CE} = 5 V, I_C = 1 A	8	—	28	—
		$h_{FE\,(2)}$	V_{CE} = 5 V, I_C = 6 A	5	—	9	
Collector-Emitter Saturation Voltage		$V_{CE\,(sat)}$	I_C = 6 A, I_B = 1.2 A	—	—	5	V
Base-Emitter Saturation Voltage		$V_{BE\,(sat)}$	I_C = 6 A, I_B = 1.2 A	—	0.9	1.2	V
Forward Voltage (Damper Diode)		$-V_F$	I_F = 8 A	—	1.6	2.0	V
Transition Frequency		f_T	V_{CE} = 10 V, I_C = 0.1 A	—	2	—	MHz
Collector Output Capacitance		C_{ob}	V_{CB} = 10 V, I_E = 0, f = 1 MHz	—	155	—	pF
Switching Time (Fig.1)	Storage Time	t_{stg}	I_{CP} = 6 A, $I_{B1\,(end)}$ = 1.5 A	—	9	12	μs
	Fall Time	t_f	f_H = 15.75 kHz	—	0.3	0.7	

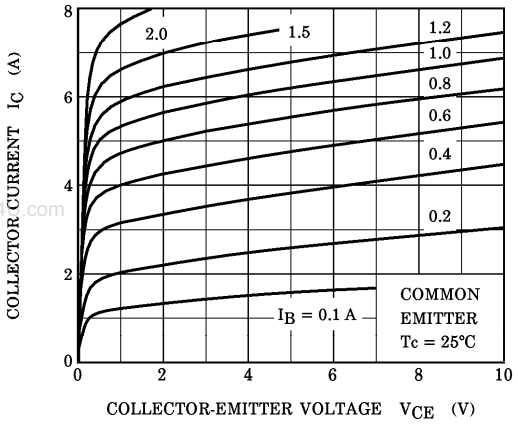
Fig.1 Switching time test circuit



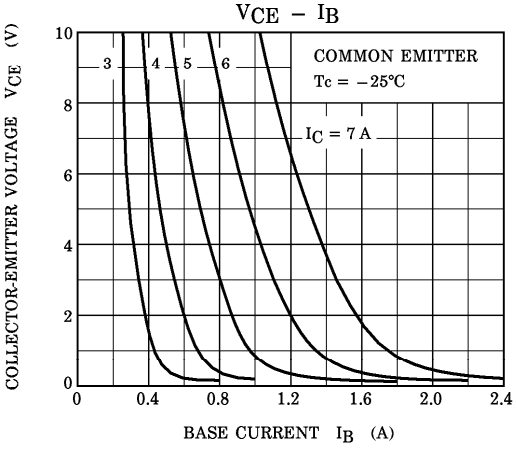
Base Current Gradient

$$dI_B/dt = \frac{I_{B1} + I_{B2}}{t_{stg}} \ (A/\mu s)$$

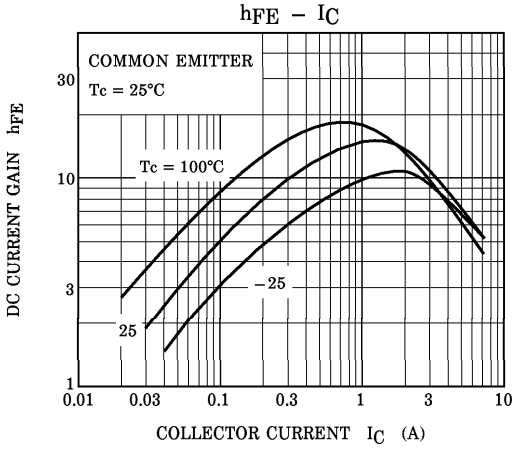
I_C – V_{CE}



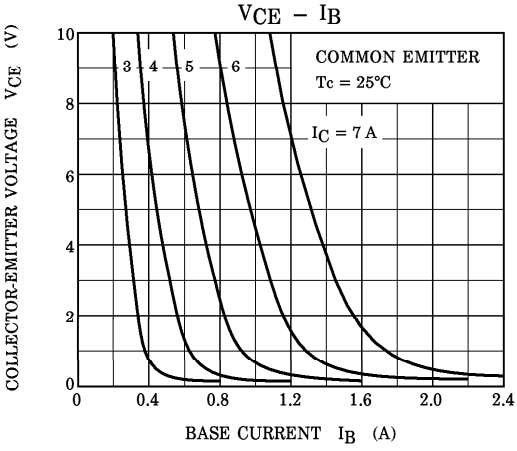
V_{CE} – I_B



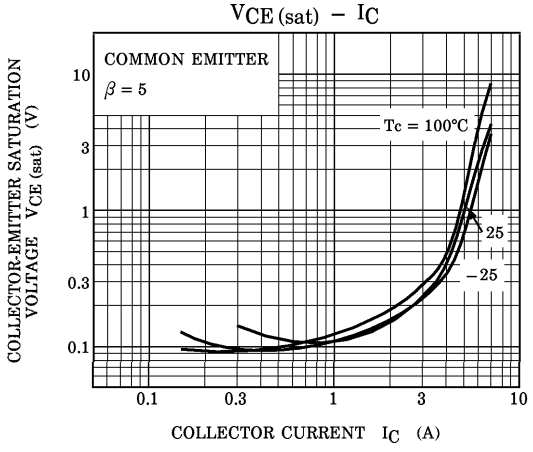
h_{FE} – I_C



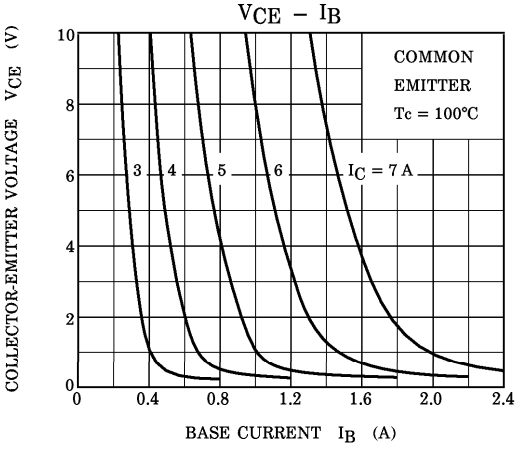
V_{CE} – I_B



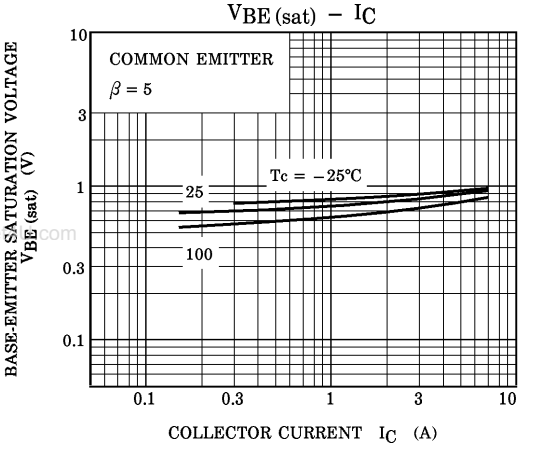
$V_{CE\,(sat)}$ – I_C



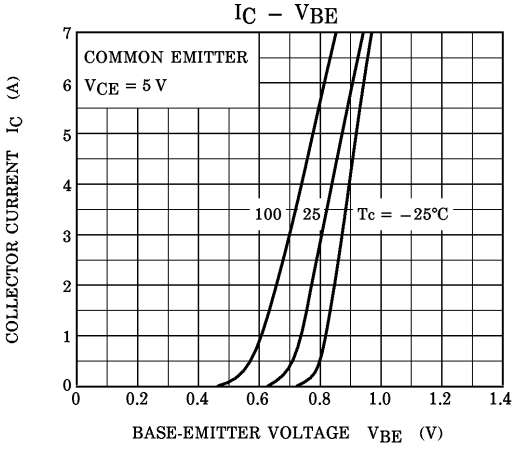
V_{CE} – I_B



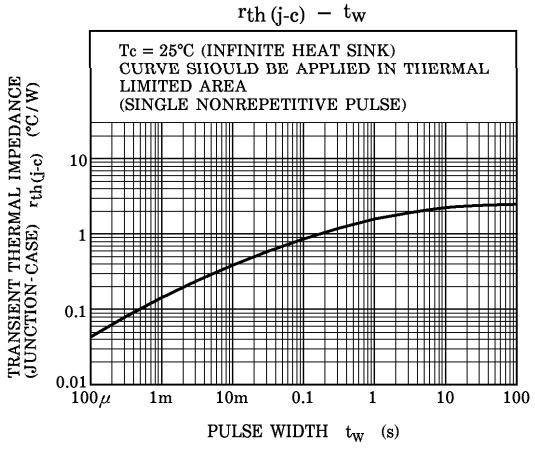
$V_{BE\,(sat)}$ – I_C



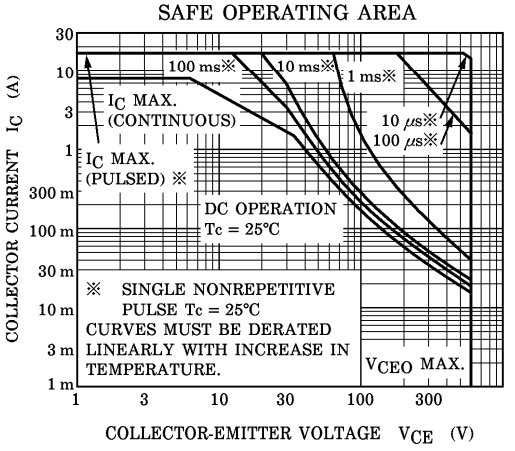
I_C – V_{BE}



$r_{th\,(j\text{-}c)}$ – t_w



SAFE OPERATING AREA



P_C – Tc