

## 19A, 100V, 0.200 Ohm, P-Channel Power MOSFET

This is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. It is a P-Channel enhancement mode silicon gate power field effect transistor designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17521.

## Ordering Information

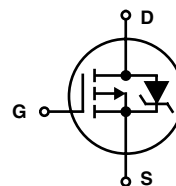
PART NUMBER	PACKAGE	BRAND
IRFP9140	TO-247	IRFP9140

NOTE: When ordering, use the entire part number.

## Features

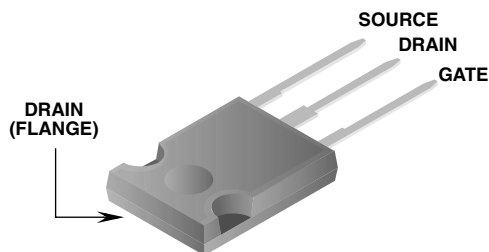
- 19A, 100V
- $r_{DS(ON)} = 0.200\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

## Symbol



## Packaging

JEDEC STYLE TO-247



# IRFP9140

## Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$ , Unless Otherwise Specified

	IRFP9140	UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DS}$ -100	V
Drain to Gate Voltage ( $R_{GS} = 20\text{k}\Omega$ ) (Note 1) . . . . .	$V_{DGR}$ -100	V
Continuous Drain Current . . . . .	$I_D$ -19	A
$T_C = 100^{\circ}\text{C}$ . . . . .	$I_{DM}$ -12	A
Pulsed Drain (Note 3) . . . . .	$I_{DM}$ -76	A
Gate to Source Voltage . . . . .	$V_{GS}$ $\pm 20$	V
Maximum Power Dissipation . . . . .	$P_D$ 150	W
Linear Derating Factor . . . . .	1.2	$\text{W}/^{\circ}\text{C}$
Single Pulse Avalanche Energy Rating . . . . .	$E_{as}$ 960	mJ
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$ -55 to 150	$^{\circ}\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s. . . . .	$T_L$ 300	$^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	$T_{pkg}$ 260	$^{\circ}\text{C}$

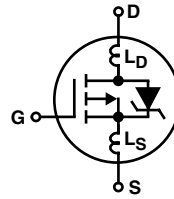
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1.  $T_J = 25^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

## Electrical Specifications $T_C = 25^{\circ}\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$ , (Figure 10)	-100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-2.0	-	-4.0	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}, T_J = 125^{\circ}\text{C}$	-	-	250	$\mu\text{A}$
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)} \text{ MAX}, V_{GS} = -10\text{V}$	-19	-	-	A
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$V_{GS} = -10\text{V}, I_D = -10\text{A}$ , (Figures 8, 9)	-	0.14	0.20	$\Omega$
Forward Transconductance (Note 2)	$g_{fs}$	$V_{DS} \leq -50\text{V}, I_D = -10\text{A}$ , (Figure 12)	5.3	7.9	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = -50\text{V}, I_D \approx -19\text{A}, R_G = 9.1\Omega, R_L = 2.5\Omega$ , $V_{GS} = -10\text{V}$ , (Figures 17, 18) MOSFET Switching Times Are Essentially Independent of Operating Temperature	-	16	20	ns
Rise Time	$t_r$		-	65	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	47	70	ns
Fall Time	$t_f$		-	28	70	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	$V_{GS} = -10\text{V}, I_D = -19\text{A}, V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ , $I_{G(REF)} = -1.5\text{mA}$ (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature	-	37	55	nC
Gate to Source Charge	$Q_{gs}$		-	8.7	-	nC
Gate to Drain "Miller" Charge	$Q_{gd}$		-	22	-	nC
Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{V}, V_{DS} = -25\text{V}, f = 1.0\text{MHz}$ , (Figure 11)	-	1200	-	pF
Output Capacitance	$C_{OSS}$		-	570	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	160	-	pF
Internal Drain Inductance	$L_D$	Measured Between Contact Screw on Header That Is Closer to Source and Gate Pins and Center of Die	-	5.0	-	nH
Internal Source Inductance	$L_S$	Measured From the Source Pin, 6mm (0.25in) From Header and Source Bonding Pad	-	13	-	nH
Junction to Case	$R_{\theta JC}$		-	-	0.83	$^{\circ}\text{C}/\text{W}$
Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	$^{\circ}\text{C}/\text{W}$



## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	$I_{SD}$	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode	-	-	-19	A
Pulse Source to Drain Current (Note 3)	$I_{SDM}$		-	-	-76	A
Source to Drain Diode Voltage (Note 2)	$V_{SD}$	$T_J = 25^\circ\text{C}$ , $I_{SD} = -19\text{A}$ , $V_{GS} = 0\text{V}$ , (Figure 13)	-	-	-1.5	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}$ , $I_{SD} = -18\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	210	-	ns
Reverse Recovery Charge	$Q_{RR}$	$T_J = 25^\circ\text{C}$ , $I_{SD} = -18\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	2.0	-	$\mu\text{C}$

## NOTES:

- Pulse test: pulse width  $\leq 80\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Repetitive rating: pulse width limited by Maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
- $V_{DD} = 50\text{V}$ , start  $T_J = 25^\circ\text{C}$ ,  $L = 4.2\text{mH}$ ,  $R_G = 25\Omega$ , peak  $I_{AS} = 19\text{A}$ . See Figures 15, 16.

## Typical Performance Curves Unless Otherwise Specified

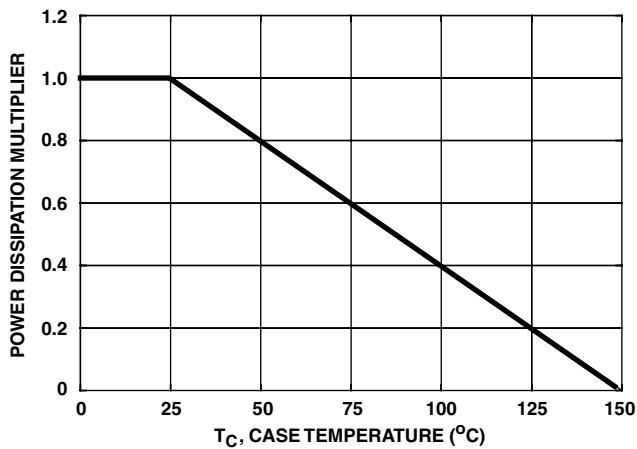


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

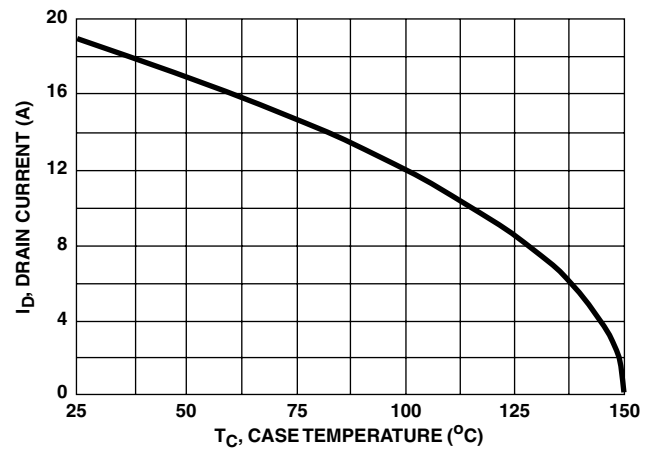


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

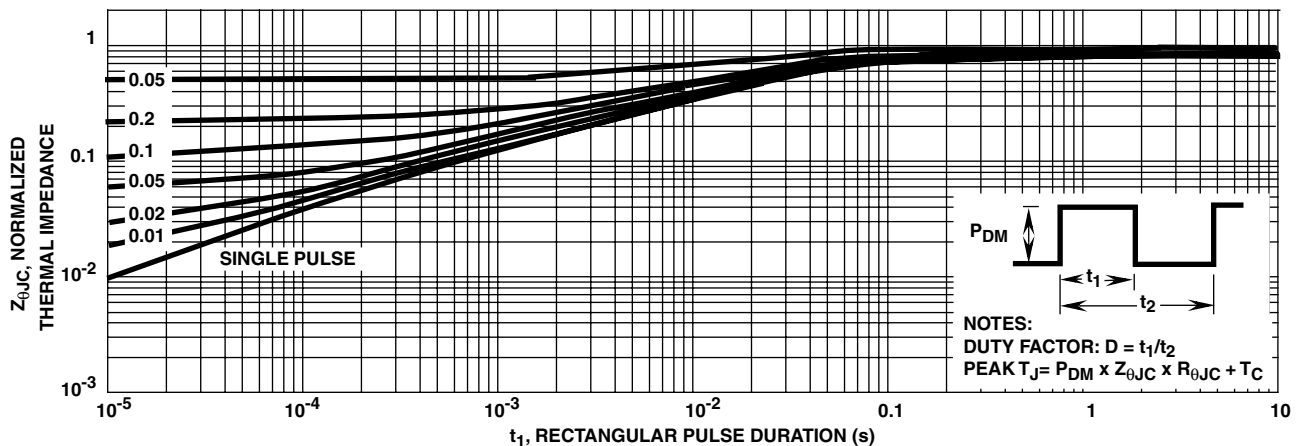


FIGURE 3. NORMALIZED TRANSIENT THERMAL IMPEDANCE

# Typical Performance Curves Unless Otherwise Specified (Continued)

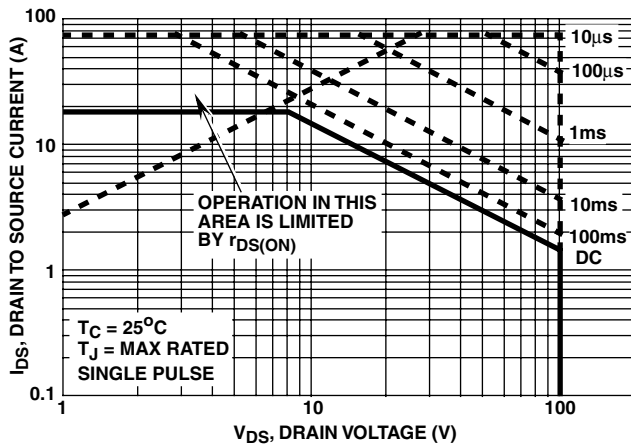


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

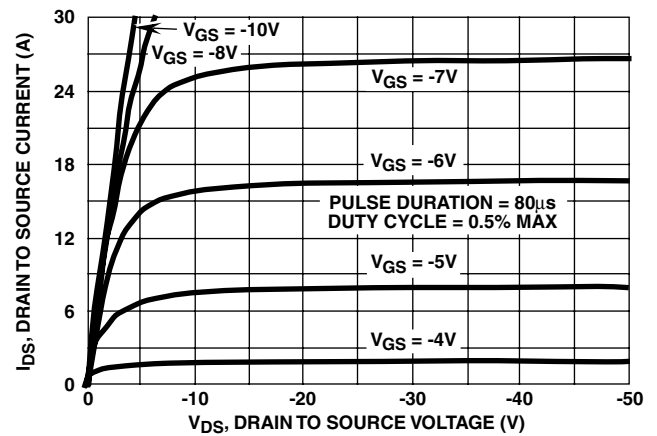


FIGURE 5. OUTPUT CHARACTERISTICS

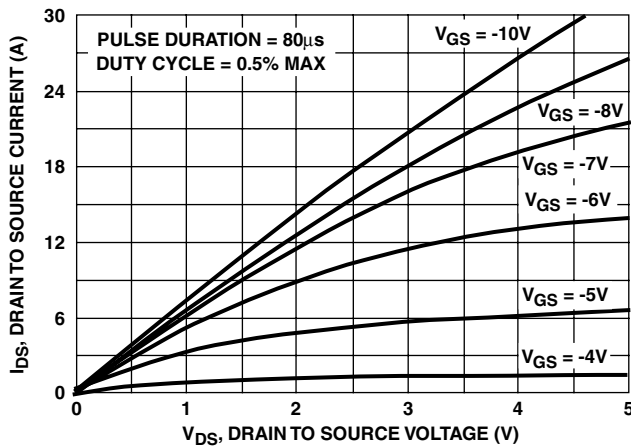


FIGURE 6. SATURATION CHARACTERISTICS

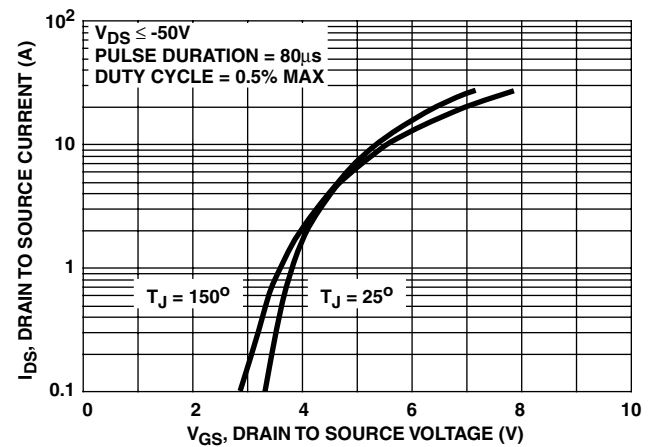


FIGURE 7. TRANSFER CHARACTERISTICS

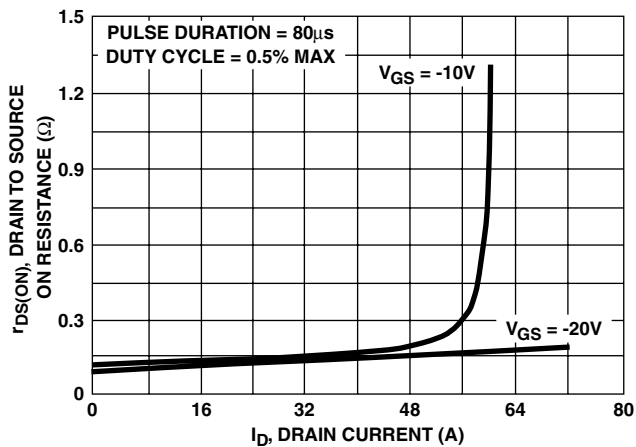


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

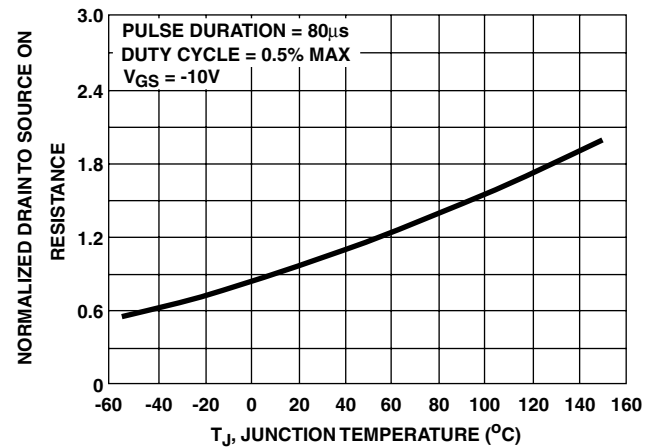


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

**Typical Performance Curves** Unless Otherwise Specified (Continued)

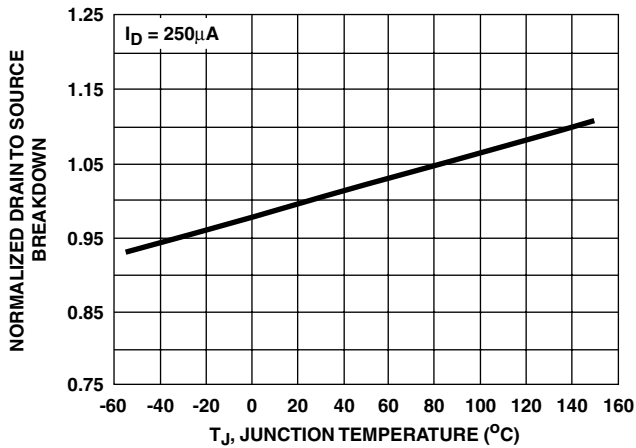


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

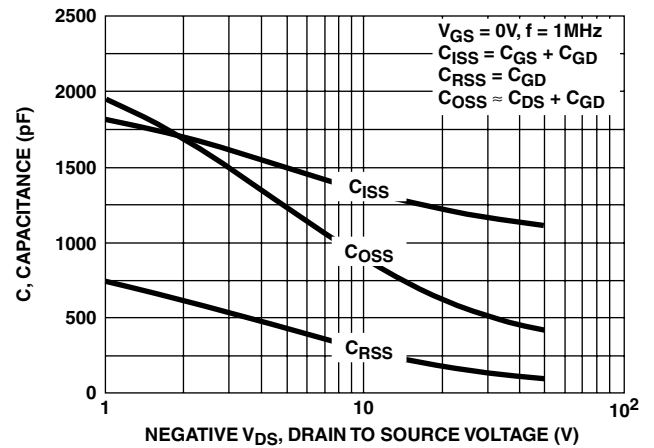


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

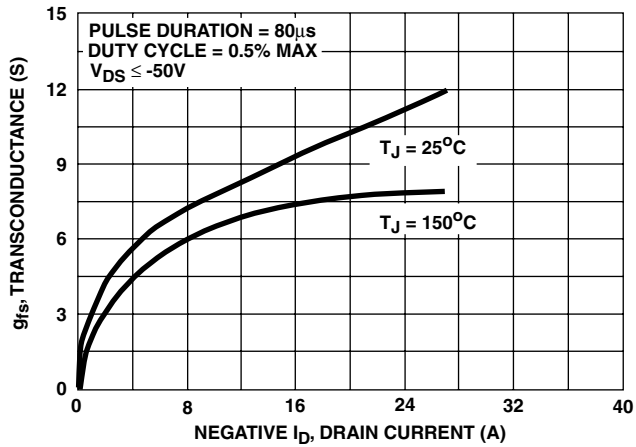


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

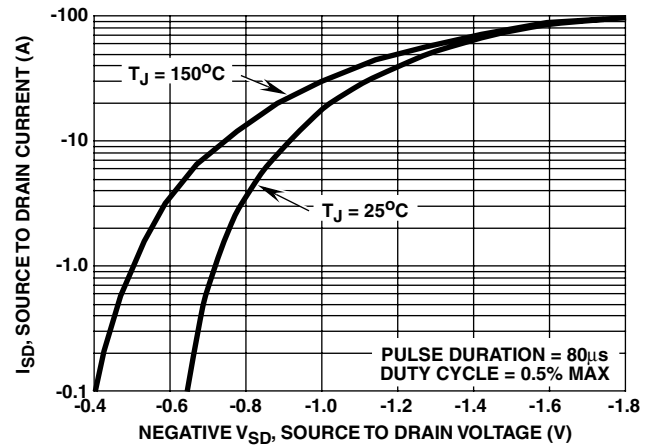


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

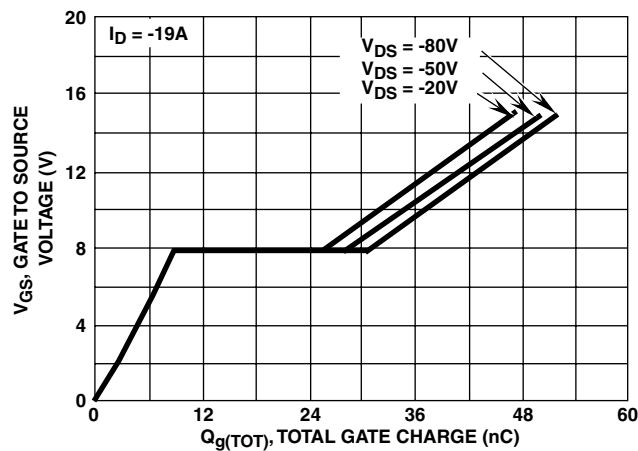


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

## Test Circuits and Waveforms

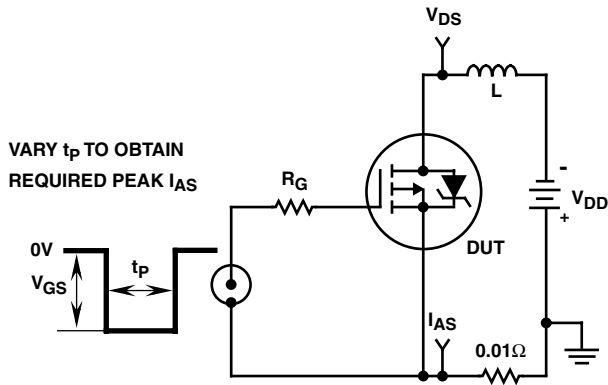


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

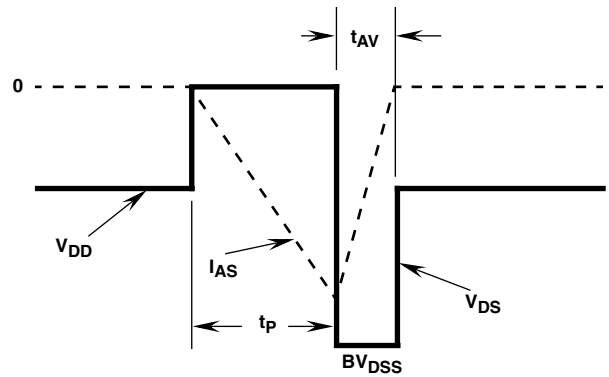


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

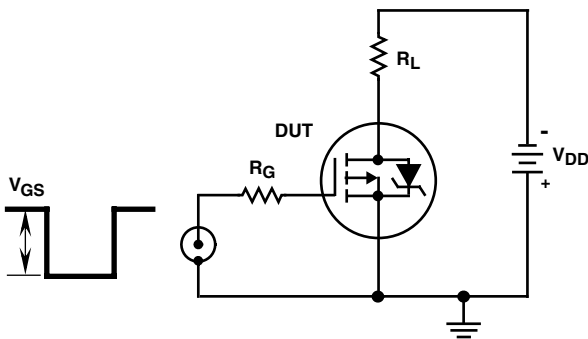


FIGURE 17. SWITCHING TIME TEST CIRCUIT

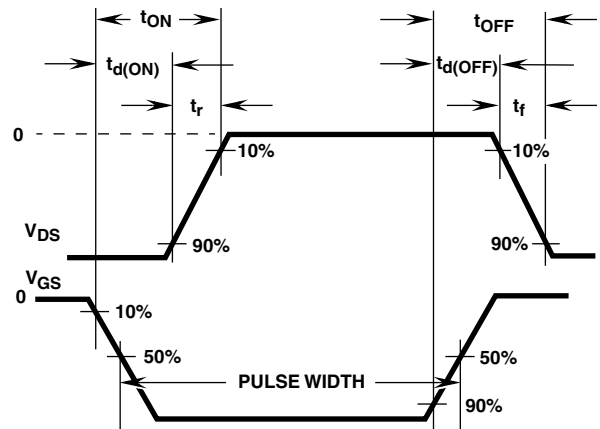


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

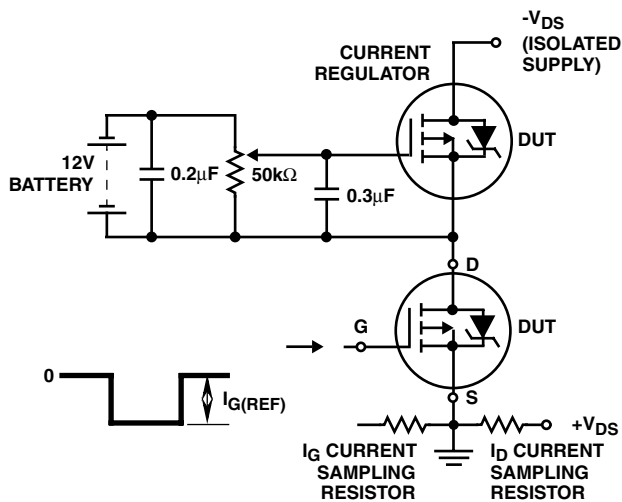


FIGURE 19. GATE CHARGE TEST CIRCUIT

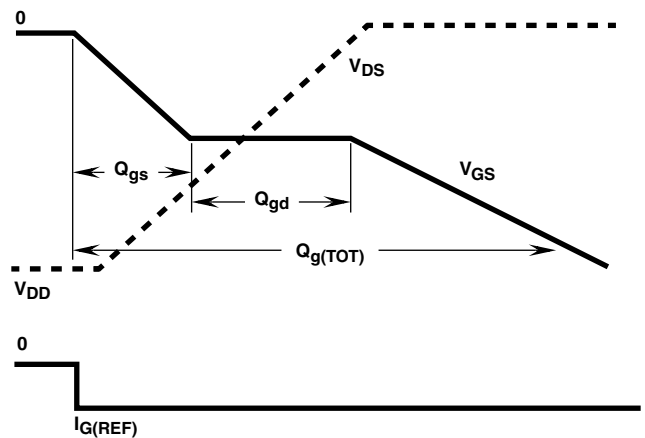


FIGURE 20. GATE CHARGE WAVEFORMS

## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST®	OPTOLOGIC™	SMART START™	VCX™
Bottomless™	FASTr™	OPTOPLANAR™	STAR*POWER™	
CoolFET™	FRFET™	PACMAN™	Stealth™	
CROSSVOLT™	GlobalOptoisolator™	POP™	SuperSOT™-3	
DenseTrench™	GTO™	Power247™	SuperSOT™-6	
DOMETM	HiSeC™	PowerTrench®	SuperSOT™-8	
EcoSPARK™	ISOPLANAR™	QFET™	SyncFET™	
E <sup>2</sup> CMOS™	LittleFET™	QST™	TinyLogic™	
EnSigna™	MicroFET™	QT Optoelectronics™	TruTranslation™	
FACT™	MicroPak™	Quiet Series™	UHC™	
FACT Quiet Series™	MICROWIRE™	SILENT SWITCHER®	UltraFET®	

STAR\*POWER is used under license

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. H4