



5 Amps, 800 Volts N-CHANNEL POWER MOSFET

DESCRIPTION

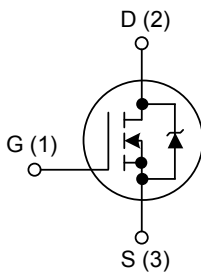
The UTC **5N80** is a N-channel enhancement mode Power MOSFET. It use UTC advanced technology to provide avalanche rugged technology and low gate charge.

It can be applied in high current, high speed switching, switch mode power supplies (SMPS), consumer and industrial lighting, DC-AC inverters for welding equipment and uninterruptible power supply(UPS).

FEATURES

- * $R_{DS(on)}$: 1.8 Ω (TYP.)
- * Avalanche rugged technology
- * Low input capacitance
- * Low gate charge
- * Application oriented characterization

SYMBOL

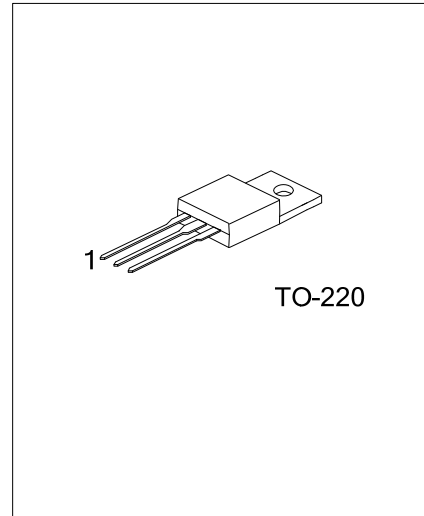


ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
5N80L-TA3-T	5N80G-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

5N80L-TA3-T	(1)Packing Type	(1) T: Tube
	(2)Package Type	(2) TA3: TO-220
	(3)Lead Free	(3) G: Halogen Free, L: Lead Free



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage	$V_{GS}=0$	V_{DS}	800	V
Gate-Source Voltage		V_{GS}	± 30	V
Drain-Gate Voltage	$R_{GS}=20\text{k}\Omega$	V_{DGR}	800	V
Drain Current (Continuous)	Continuous	I_D	5.5	A
	Pulsed (Note 2)	I_{DM}	20	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	320	mJ
Total Dissipation		P_D	125	W
Derating Factor			1	W/ $^{\circ}\text{C}$
Operation Junction Temperature		T_J	150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-65~150	$^{\circ}\text{C}$

Notes : Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction-ambient	θ_{JA}	62.5	$^{\circ}\text{C}/\text{W}$
Junction-Case	θ_{JC}	1	$^{\circ}\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	800			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =Max Rating			250	μA
			V _{DS} = Max Rating × 0.8, T _C =125°C			1000	
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V			+100	nA
	Reverse		V _{GS} =-20V			-100	nA
ON CHARACTERISTICS (Note 1)							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	3		5	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =2.5A		1.8	2.6	Ω
			V _{GS} =10V, I _D =2.5A, T _C =100°C			4	
On State Drain Current		I _{D(ON)}	V _{DS} >I _{D(ON)} ×R _{DS(ON)} max, V _{GS} =10V	5			A
Forward Transconductance (Note 1)		g _{FS}	V _{DS} >I _{D(ON)} ×R _{DS(ON)} max, I _D =2.5A	2	4		S
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		1190	1450	pF
Output Capacitance		C _{OSS}			165	200	pF
Reverse Transfer Capacitance		C _{RSS}			70	85	pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{GS} =10V, V _{DD} =500V, I _D =6A		75	95	nC
Gate to Source Charge		Q _{GS}			9		nC
Gate to Drain Charge		Q _{GD}			33		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =400V, I _D =2.5A, R _G =50Ω		50	65	ns
Rise Time		t _R	V _{GS} =10V (See test circuit, Fig. 3)		85	105	ns
Turn-OFF Delay Time		t _{D(OFF)}	V _{DD} =640V, I _D =5.5A, R _G =50Ω V _{GS} =10V (See test circuit, Fig. 5)		120	150	ns
Fall-Time		t _F			30	40	ns
Cross-Over Time		t _C			160	200	ns
Turn-On Current Slope		(di/dt) _{on}	V _{DD} =640V, I _D =5.5A, R _G =50Ω V _{GS} =10V (See test circuit, Fig. 5)		200		A/μs
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _{SD} =5.5A, V _{GS} =0V			2	V
Reverse Recovery Time		t _{RR}	I _{SD} =5.5A, di/dt=100A/μs,		700		ns
Reverse Recovery Charge		Q _{RR}	V _{DD} =80V, T _J =150°C		7.7		nC
Reverse Recovery Current		I _{RRM}	(See test circuit, Fig. 5)		22		A
Source-Drain Current		I _{SD}				5.5	A
Source-Drain Current (Pulsed) (Note 1)		I _{SDM}				20	A

Notes: 1. Pulsed: Pulse duration=300μs, duty cycle 1.5%.

2. Pulse width limited by safe operating area.

3. Starting T_J=25°C, I_D=I_{AR}, V_{DD}=50V

■ SWITCHING TIME TEST CIRCUIT

Fig. 1 Unclamped Inductive Load Test Circuits

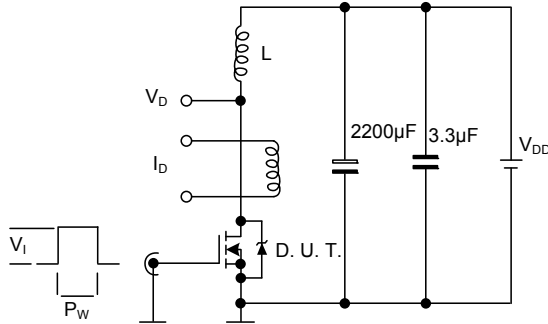


Fig. 2 Unclamped Inductive Waveforms

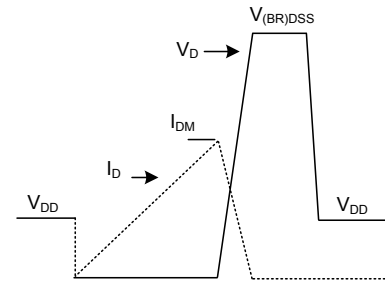


Fig. 3 Switching Times Test Circuits For Resistive Load

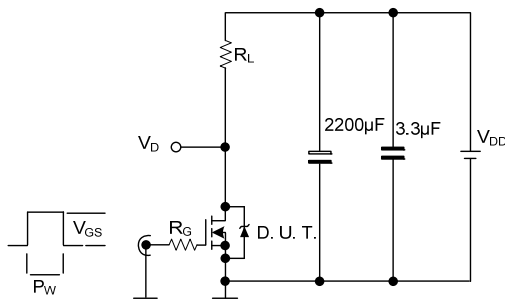


Fig. 4 Gate Charge Test Circuit

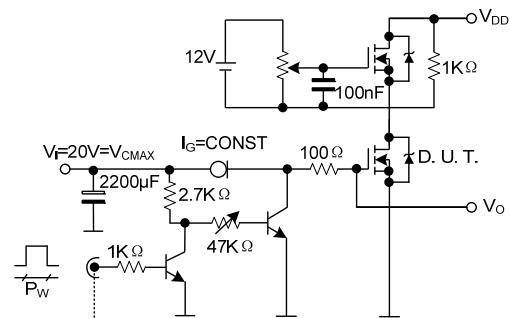
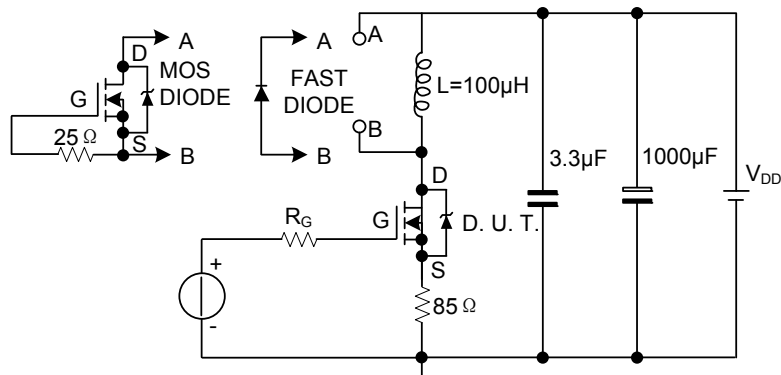


Fig. 5 Test Circuit For Inductive Load Switching And Diode Reverse Recovery Time



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