DATA SHEET

BST86
N-channel enhancement mode vertical D-MOS transistor

Product specification
File under Discrete Semiconductors, SC13b

April 1995

Philips Semiconductors

PHILIPS

N-channel enhancement mode vertical D-MOS transistor

BST86

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in SOT89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

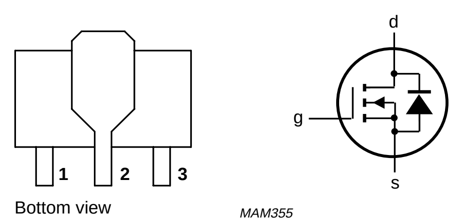
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance				
I_D = 15 mA; V_{GS} = 3 V	$R_{DS(on)}$	typ.	7	Ω
		max.	10	Ω
Transfer admittance				
I_D = 300 mA; V_{DS} = 15 V	$\lvert Y_{fs} \rvert$	typ.	250	mS

PINNING - SOT89

1 = source
2 = drain
3 = gate

PIN CONFIGURATION



Marking: K0

Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		–65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on a ceramic substrate of 2.5 cm^2 and thickness of 0.7 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
I_D = 100 µA; V_{GS} = 0	$V_{(BR)DSS}$	min.	180	V
Drain-source leakage current				
V_{DS} = 120 V; V_{GS} = 0	I_{DSS}	max.	10	µA
Gate-source leakage current				
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage				
I_D = 100 µA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.7	V
		max.	2.7	V
Drain-source ON-resistance				
I_D = 15 mA; V_{GS} = 3 V	$R_{DS(on)}$	typ.	7	Ω
		max.	10	Ω
I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	6	Ω
Transfer admittance				
I_D = 300 mA; V_{DS} = 15 V	$\lvert Y_{fs} \rvert$	typ.	250	mS
Input capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	50	pF
		max.	65	pF
Output capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	20	pF
		max.	30	pF
Feedback capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	6	pF
		max.	10	pF
Switching times (see as 2 and 3)				
I_D = 300 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	max.	10	ns
	t_{off}	max.	15	ns

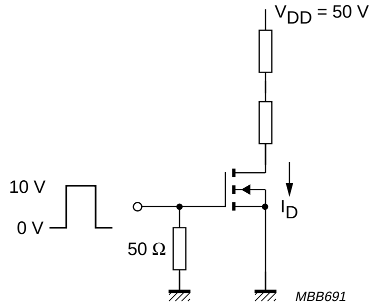


Fig.2 Switching times test circuit.

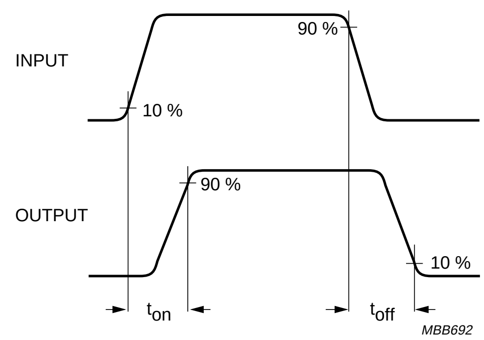
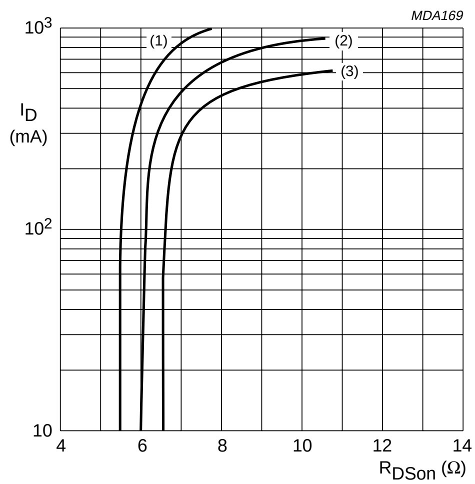


Fig.3 Input and output waveforms.



(1) V_{GS} = 10 V.
(2) V_{GS} = 5 V.
(3) V_{GS} = 4 V.

Fig.4 T_j = 25 °C; typical values.

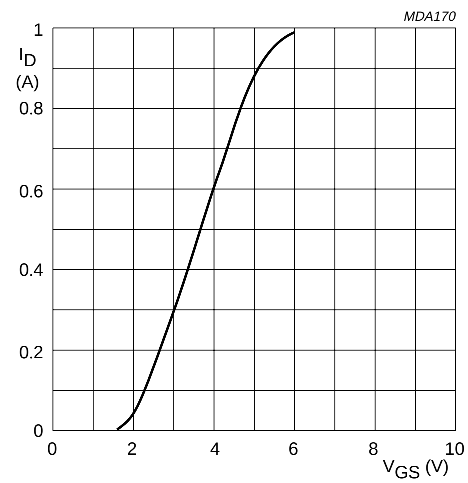
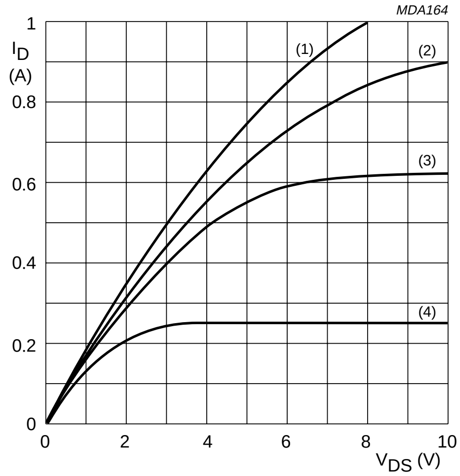


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typ. values.



(1) V_{GS} = 10 V.
(2) V_{GS} = 5 V.
(3) V_{GS} = 4 V.
(4) V_{GS} = 3 V.

Fig.6 T_j = 25 °C; typical values.

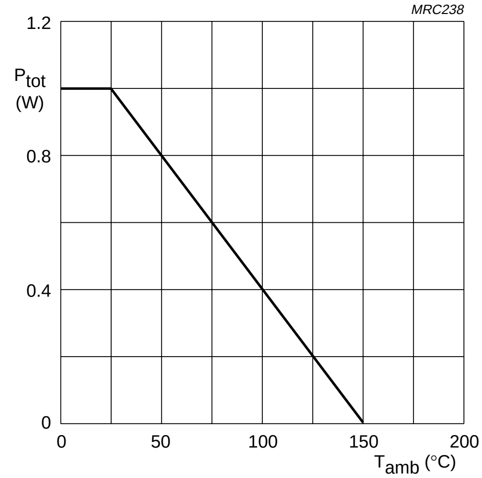
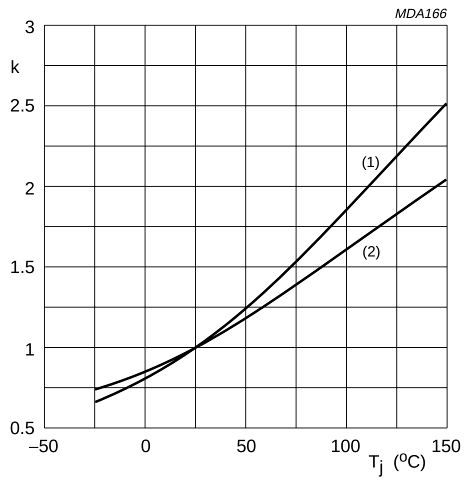


Fig.7 Power derating curve.



(1) I_D = 300 mA; V_{GS} = 10 V.
(2) I_D = 15 mA; V_{GS} = 3 V.

Fig.8

$$k = \frac{R_{DS\ on} \text{ at } T_j}{R_{DS\ on} \text{ at } 25\ °C};$$

typcial values.

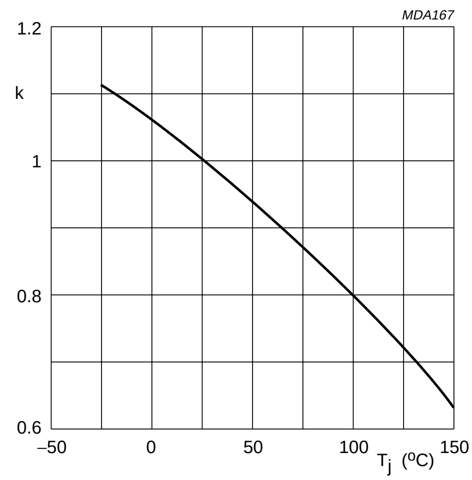
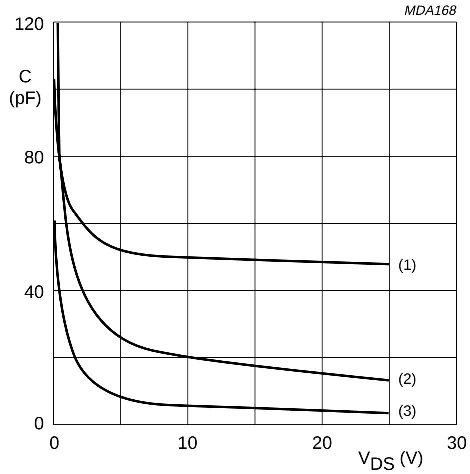


Fig.9

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 01. mA; typical values.



(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

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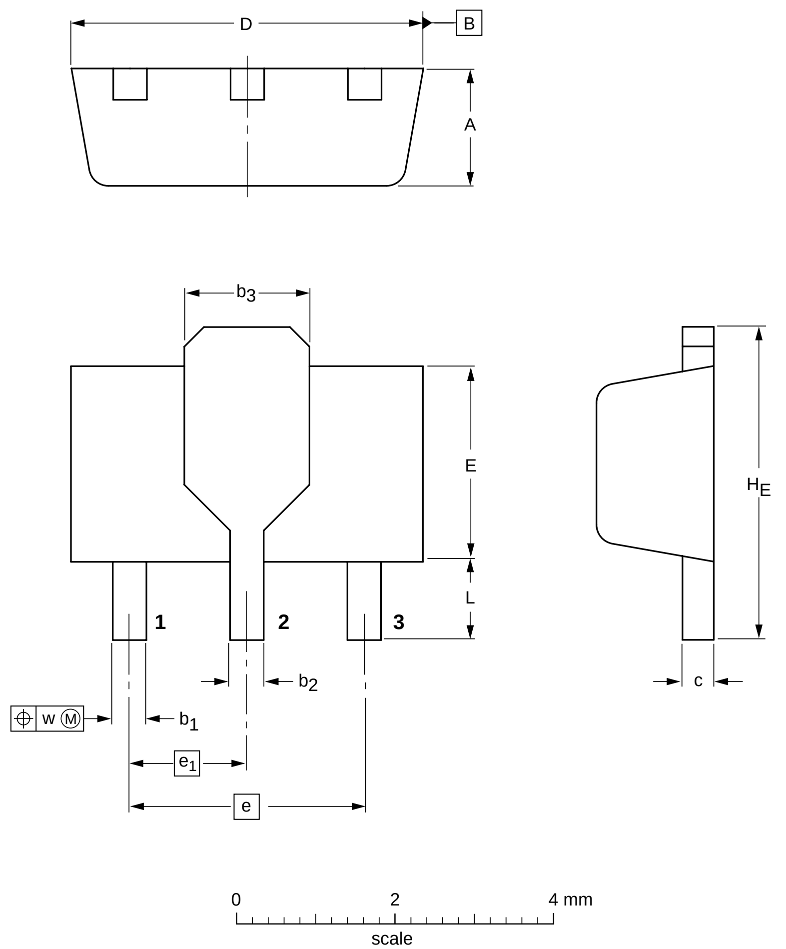
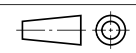
PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 3 leads **SOT89**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_1	b_2	b_3	c	D	E	e	e_1	H_E	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT89						97-02-28

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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